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(54)名 稱：供顯示裝置用之驅動方法及驅動電路

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[57]申請專利範圍：

1. 一種驅動顯示裝置之方法，顯示裝置包含許多圖素，許多掃描線及許多資料線，各圖素經一開關元件連至一掃描線及一資料線，

該方法包含步驟如下：

a)將一振盪電壓信號加至各資料線，振盪電壓在第一圖素充電期間週期性地振盪；

b)將第一掃描信號加至第一掃描線，第一掃描信號界定一第一時序，其中連至第一圖素的第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF；以及

c)將第二掃描信號加至鄰接於第一掃描線的第二掃描線，第二掃描信號界定一第二時序，其中連至鄰接第一圖素的第二圖素之第二開關元件的狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第二時序與第一時序不同。

2. 根據申請專利範圍第1項之方法，其中第二圖素在資料線的縱向上鄰接第一圖素。

3. 根據申請專利範圍第1項之方法，並含對各掃描線交替重複步驟b)與c)的步驟。

4. 根據申請專利範圍第1項之方法，其中各圖素包含一組副圖素，且其中各資料線包含一組副資料線，各組副資料線連至各組副圖素。

5. 一種驅動顯示裝置之方法，顯示裝置包含許多圖素、許多掃描線及許多資料線，各圖素經一開關元件連至一掃描線及一資料線，

該方法包含步驟如下：

a)將一振盪電壓信號加至各資料線，振盪電壓在第一圖素充電期間週期性地振盪；

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b)將第一掃描信號加至第一畫面中第一掃描線，第一掃描信號界定一第一時序，其中連至第一圖素之第一開關元件的狀態在振盪電壓信號的一個振盪週期內從ON變成OFF；以及

c)將第二掃描信號加至與第一畫面不同的第二畫面中第一掃描線，第二掃描信號界定一第二時序，其中連至第一圖素的第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第二時序與第一時序不同。

6. 根據申請專利範圍第5項之方法，其中第二畫面在第一畫面之後。

7. 根據申請專利範圍第5項之方法，並含對各畫面交替重複步驟b)與c)之步驟。

8. 根據申請專利範圍第5項之方法，並含步驟

d)將一第三掃描信號加至與第二畫面不同的第三畫面中第一掃描線，第三掃描線信號界定一第三時序，其中連至第一圖素的第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第三時序與第二時序不同。

9. 根據申請專利範圍第8項之方法，並含對各畫面週期性重複步驟b)、c)與d)之步驟。

10. 根據申請專利範圍第5項之方法，並含步驟

e)將第四掃描信號加至鄰接於第一掃描線之第二掃描線，第四掃描線信號界定一第四時序，其中連至鄰接於第一圖素的第二圖素之第二開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第四時序與第一時序不同。

11. 根據申請專利範圍第10項之方法，並

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含對各掃描線交替重複步驟b)與e)之步驟。

12. 根據申請專利範圍第10項之方法，其中步驟e)中第四時序實質上等於步驟c)中第二時序。

13. 根據申請專利範圍第10項之方法，並含步驟

f)將第五掃描信號加至鄰接於第二掃描線的第三掃描線，第五掃描信號界定一第五時序，其中連至鄰接第二圖素之第三圖素的第三開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第五時序與第一時序不同。

14. 根據申請專利範圍第13項之方法，並含對各掃描線週期性重複步驟b)、e)與f)之步驟。

15. 根據申請專利範圍第13項之方法，其中步驟e)中第四時序實質上等於步驟c)中第二時序，且其中步驟f)中第五時序實質上等於步驟d)中第三時序。

16. 根據申請專利範圍第5項之方法，其中各圖素包含一組副圖素，且其中各資料線包含一組副資料線，各組副資料線連至各組副圖素。

17. 一種驅動顯示裝置的驅動電路，顯示裝置包含許多圖素、許多掃描線及許多資料線，各圖素經一開關元件連至一掃描線及一資料線

該驅動電路包含：

一資料驅動器，將一振盪電壓信號加至各資料線，振盪電壓在第一圖素充電期間週期性地振盪；及

一掃描驅動器，將第一掃描信號加至第一掃描線，且將第二掃描信號加至鄰接於第一掃描線的第二掃描線，第一掃描信號界定一第一時序，其中連至第一圖素的第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第二掃描信號界定一

第二時序，其中連至鄰接於第一圖素之第二圖素的第二開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，且第二時序與第一時序不同。

18.根據申請專利範圍第17項之驅動電路，其中第二圖素在資料線的縱向上鄰接於第一圖素。

19.一種驅動顯示裝置的驅動電路，顯示裝置包含許多圖素、許多掃描線及許多資料線，各圖素經一開關元件連至一掃描線及一資料線，

該驅動電路包含：

一資料驅動器，將一振盪電壓信號加至各資料線，振盪電壓在第一圖素充電期間週期性地振盪；及

一掃描驅動器，將一掃描信號加至第一畫面中第一掃描線，並將第二掃描信號加至與第一畫面不同的第二畫面中第一掃描線，第一掃描信號界定一第一時序，其中連至第一圖素之第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第二掃描信號界定一第二時序，其中連至第一圖素的第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第二時序與第一時序不同。

20.根據申請專利範圍第19項之驅動電路，其中第二畫面在第一畫面之後。

21.根據申請專利範圍第19項之驅動電路，其中掃描驅動器並將一第三掃描信號加至與第二畫面不同之第三畫面中第一條掃描線，第三掃描信號界定一第三時序，其中連至第一圖素的第一開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第三時序與第二時序不同。

22.根據申請專利範圍第19項之驅動電路，其中掃描驅動器並將一第四掃描信號加至鄰接於第一掃描線的第二掃描線，第四掃描信號界定一第四時序，其中連至鄰接第一圖素之第二圖素的第二開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第四時序與第一時序不同。

23.根據申請專利範圍第22項之驅動電路，其中掃描驅動器並將一第五掃描信號加至鄰接第二掃描線之第三掃描線，第五掃描信號界定一第五時序，其中連至鄰接於第二圖素之第三圖素的第三開關元件之狀態在振盪電壓信號的一個振盪週期內從ON變成OFF，第五時序與第一時序不同。

圖示簡單說明：

圖1示出一在兩畫面期間改變閘OFF時序之電路構造，其根據本發明第一例子含在一驅動電路的掃描驅動器中供顯示裝置之用。

圖2A示出水平同步信號H_{sync}的波形；

圖2B示出從圖1所示電路輸出的閘時鐘GCK'之波形；以及

圖2C示出閘時鐘GCK'的上升邊緣。

圖3示出一電路構造，用以在兩條線與兩畫面期間改變閘OFF時序，其根據本發明第二例子含在一驅動電路的掃描驅動器中供顯示裝置之用。

圖4A示出水平同步信號H_{sync}的波形；

圖4B示出從圖3所示電路輸出的閘時鐘GCK'之波形；以及

圖4C示出閘時鐘GCK'的上升邊緣。

圖5爲一波形表，示出本發明可以適用的4位元驅動器之振盪電壓圖形。

圖6爲一方塊圖，示出構成3位元驅動器之衆輸出電路其中之一，採用振盪電壓法供傳統動態矩陣式液晶顯示裝置之用。

圖7示出傳統驅動器中一選擇控制器

的詳細構造。

圖8示出一脈衝信號波形，作用比爲2：1，用以在根據本發明之3位元驅動器的輸出電路中及傳統3位元驅動器的輸出電路中產生一振盪電壓。

圖9A至9D示出當從根據本發明之3位元驅動器及傳統3位元驅動器之輸出電路輸出的視頻信號資料分別爲「1」、「3」、「4」與「6」時之振盪電壓波形。

圖10概略示出一構成傳統動態矩陣式液晶顯示裝置之TFT液晶板之構造。

圖11示出TFT液晶板之配置，一上邊驅動器及一下邊驅動器配置在板上方與下方，以及板的構造。

圖12示出TFT液晶板的等效電路，用分布常數與驅動器相連。

圖13A及13B示出以集總常數表示的等效電路，其從圖12中以分布常數表示的等效電路轉換而來。

圖14示出當視頻信號資料爲「3」時，加至預定圖素之電壓波形，或是加至圖素UP1之電壓波形，圖素UP1則以最靠近驅動器之上邊驅動器驅動(或者圖素LPL，以下邊驅動器驅動，並最靠近

驅動器)，及加至圖素UPL的電壓波形，圖素UPL以上邊驅動器驅動，並最遠離驅動器(或者圖素LP1以下邊驅動器驅動，並最遠離驅動器)。

圖15示出振盪電壓的頻率與使用振盪電壓法之液晶顯示裝置中電力消耗之間的關係。

圖16示出加至圖素UP1(或LPL)及加至圖14所示圖素UPL(或LP1)之電壓波形之間的位置關係，以及加至TFT閘之閘脈衝下落時序。

圖17示出液晶顯示裝置中在液晶板屏幕上產生的細條紋。

圖18示出從3位元驅動器輸出的振盪電壓波形，以及在各個圖素之振盪電壓變化。

圖19示出振盪電壓之波形，與圖18所示者不同，從一3位元驅動器輸出，以及在各個圖素之振盪電壓變化。

圖20概略示出在各個畫面中由3位元驅動器驅動之圖素的充電電位。

圖21概略示出在各個畫面與線條中由3位元驅動器驅動之圖素的充電電位。

圖22示出本發明模範液晶顯示裝置及一傳統液晶顯示裝置所用的整個構造。

圖1

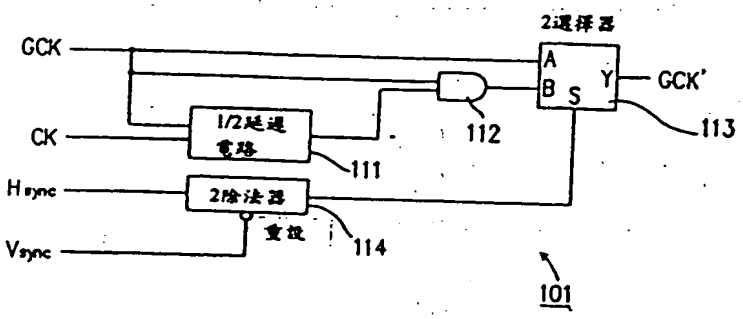


圖2A

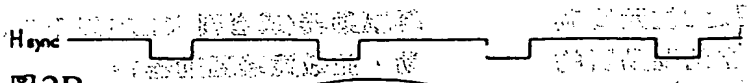


圖2B

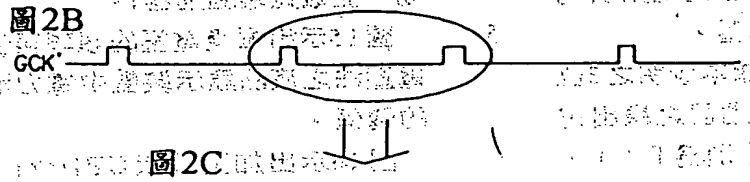


圖2C

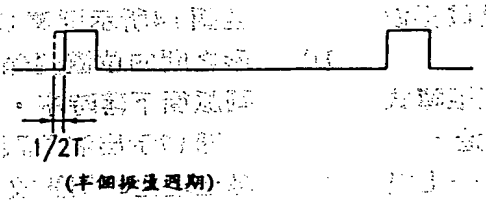


圖3

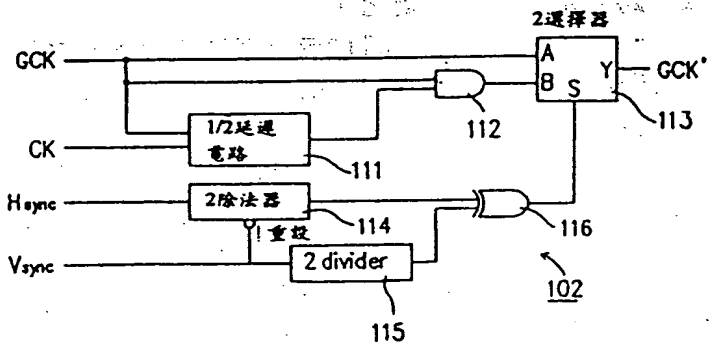


圖4A

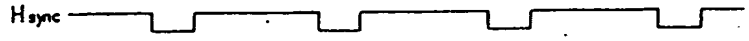


圖4B

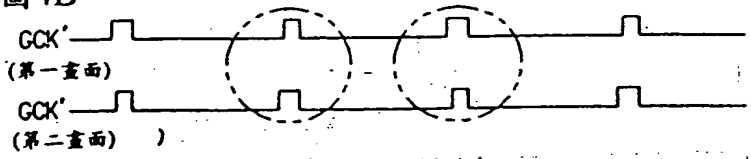


圖4C

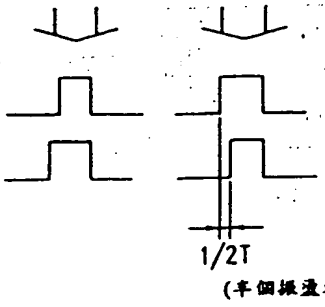
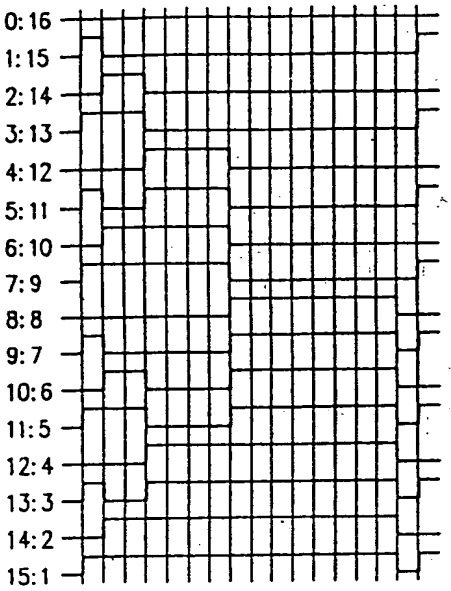


圖5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1:15
2:14
3:13
4:12
5:11
6:10
7:9
8:8
9:7
10:6
11:5
12:4
13:3
14:2
15:1

圖6

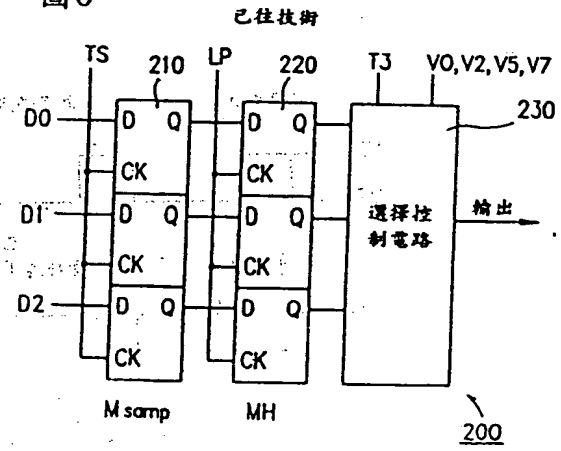

已往技術
TS
210
LP
220
T3
V0,V2,V5,V7
230
D0
D1
D2
D Q
CK
選擇控制電路
輸出
Msamp
MH
200

圖7

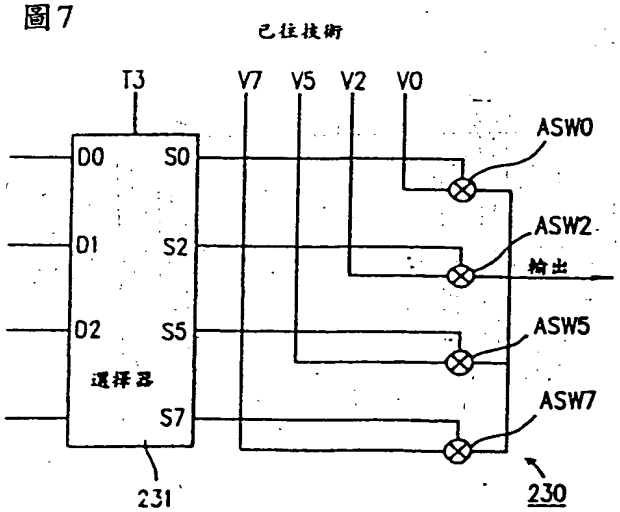

已往技術
T3
V7
V5
V2
V0
D0
D1
D2
S0
S2
S5
S7
選擇器
ASW0
ASW2
ASW5
ASW7
輸出
231
230

圖8

已往技術

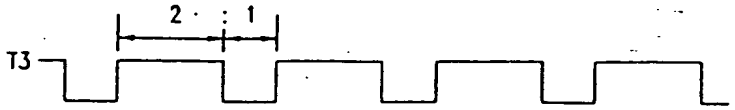


圖9A

已往技術

當資料爲「1」時之輸出波形

圖9B

已往技術

當資料爲「3」時之輸出波形

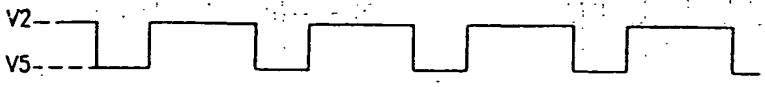


圖9C

已往技術

當資料爲「4」時之輸出波形

圖9D

已往技術

當資料爲「6」時之輸出波形

圖10

已往技術

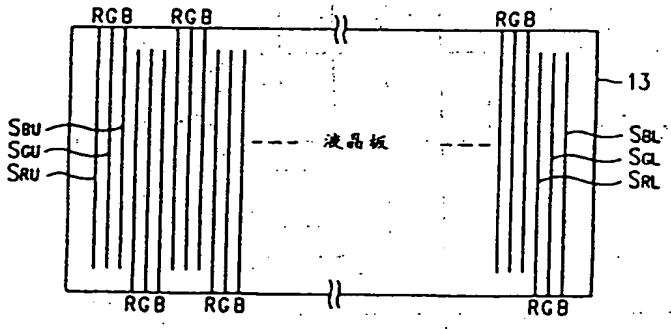


圖11

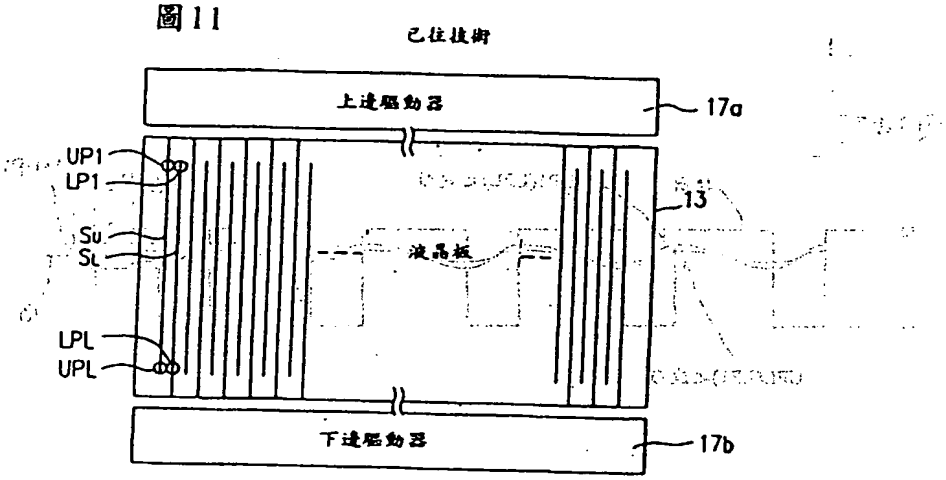


圖12

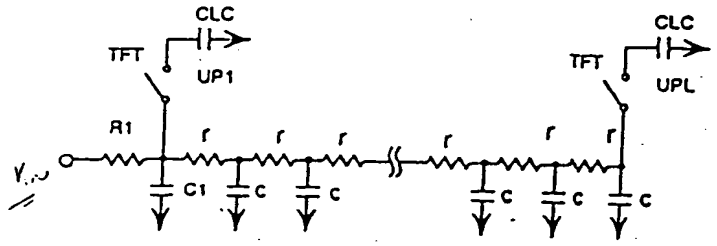


圖13A

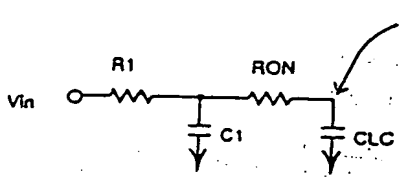


圖13B

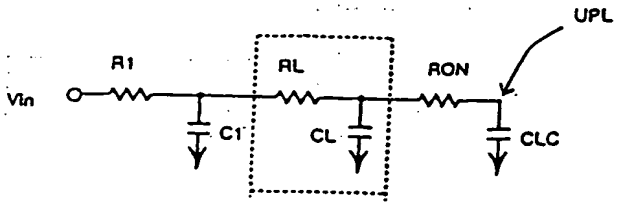


圖14

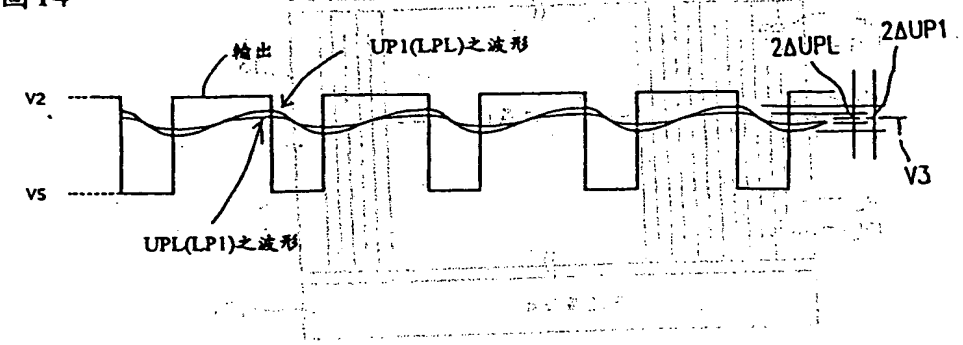

輸出
UP1(LPL)之波形
2ΔUPL
2ΔUP1
V2
V5
V3
UPL(LP1)之波形

圖15

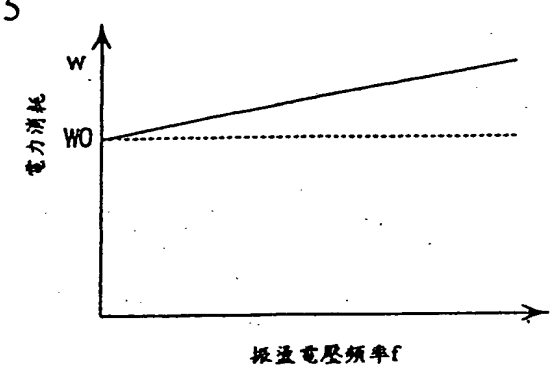

W
WO
電力消耗
振盪電壓頻率f

圖16

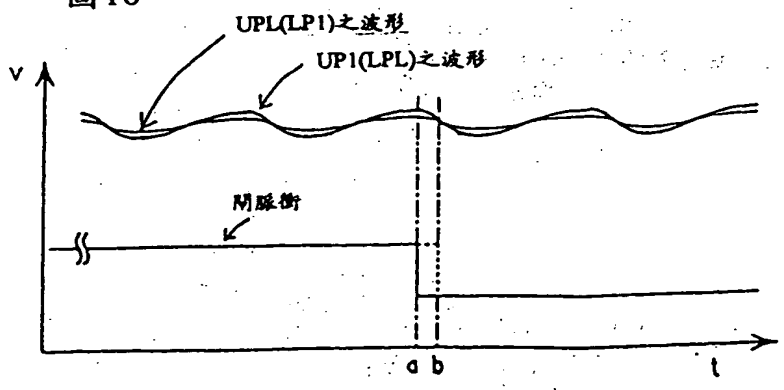

UPL(LP1)之波形
UP1(LPL)之波形
V
閉路衝
a
b
t

圖17

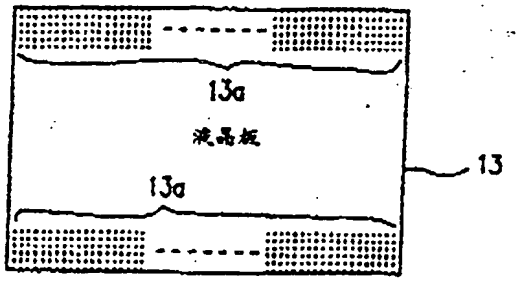

13a
液晶板
13a
13

圖18

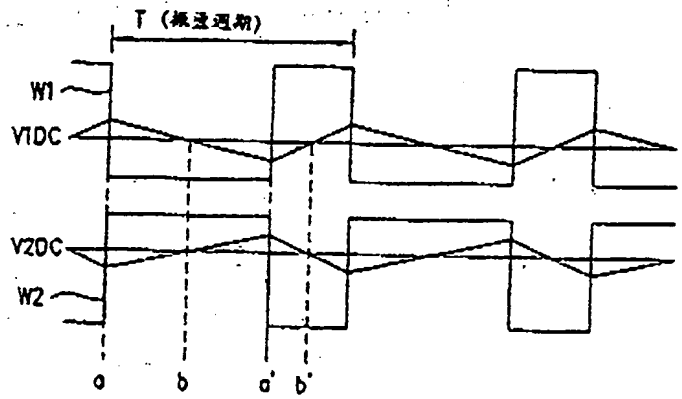
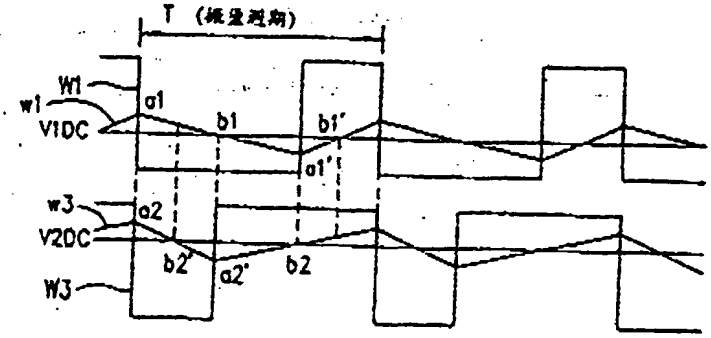

T (振盪週期)
W1
V1DC
V2DC
W2
a
b
a'
b'

圖19


T (振盪週期)
W1
w1
a1
V1DC
b1
b1'
a1'
w3
a2
V2DC
b2'
a2'
b2
W3

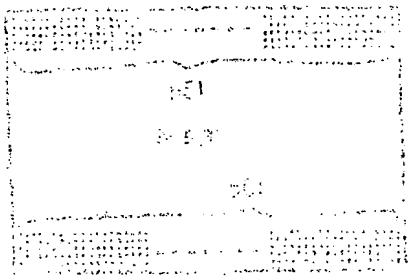


图20

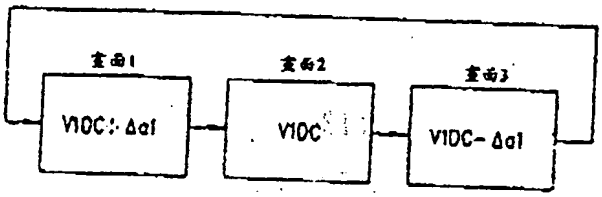

查询1
查询2
查询3
VIDC+ Δσ1
VIDC
VIDC- Δσ1

图21

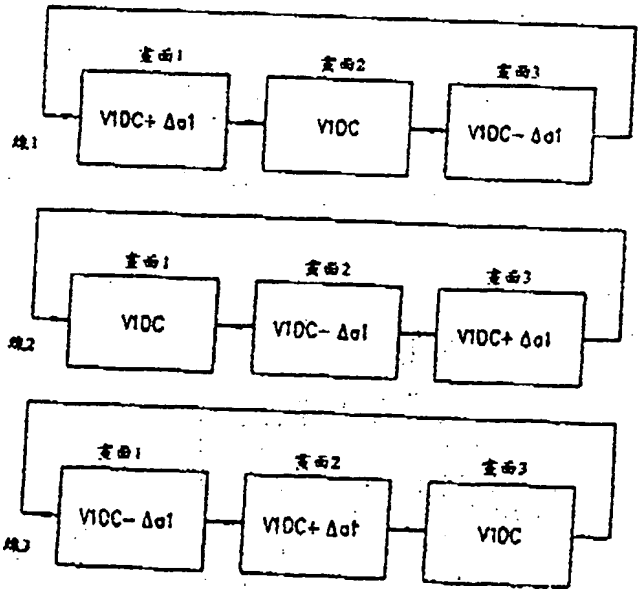
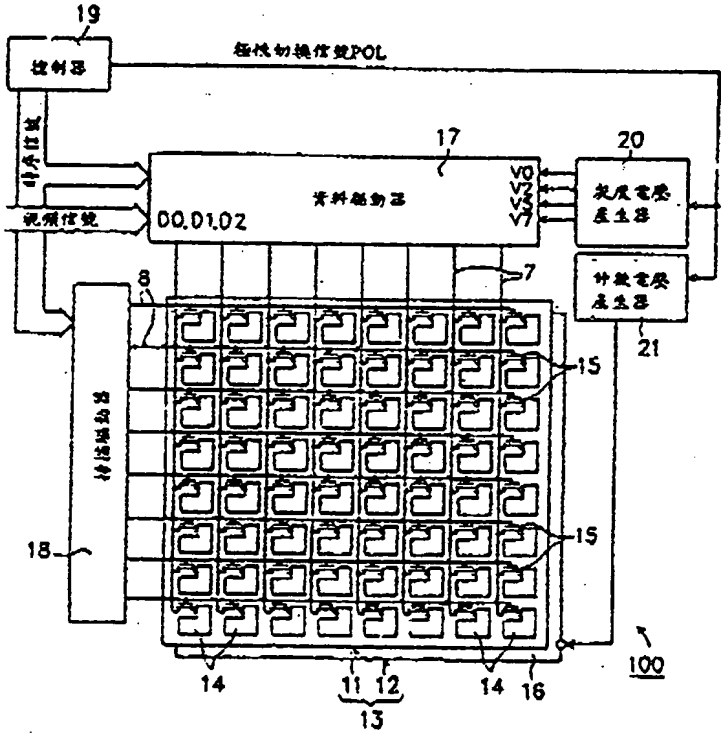

查询1
查询2
查询3
VIDC+ Δσ1
VIDC
VIDC- Δσ1
VIDC
VIDC- Δσ1
VIDC+ Δσ1
VIDC- Δσ1
VIDC+ Δσ1
VIDC

圖22


19
極性切換信號POL
17
20
D0,D1,D2
V0
V2
V5
V7
7
8
15
15
18
21
100
14
11
12
13
14
16

8411375

S95321

ABSTRACT OF THE DISCLOSURE

A method includes the steps of: a) applying an oscillating voltage signal to data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; b) applying a first scanning signal to a first scanning line, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal; and c) applying a second scanning signal to a second scanning line adjacent to the first scanning line, the second scanning signal defining a second timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second timing being different from the first timing.

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to (method) and (circuit) for driving a (flat-panel type display device) such as a liquid crystal display device. More particularly, the present invention relates to method and circuit for driving an (active-matrix) type liquid crystal display device, in which an oscillating voltage for charging a pixel is applied to data lines of the display device.

2. Description of the Related Art:

Figure 22 shows a configuration for an active-matrix type liquid crystal display device 100 which is driven by way of an (oscillating voltage method). In Figure 22, the active-matrix type liquid crystal display device 100 includes a liquid crystal panel 13 including a liquid crystal layer functioning as a display medium and a pair of substrates 11 and 12 for sandwiching the liquid crystal layer. On one substrate 11 of the liquid crystal panel 13, a plurality of pixel electrodes 14 for forming the pixels are arranged in a matrix fashion, a plurality of scanning lines 8 are provided so as to correspond to the respective rows of the pixel electrodes 14, and a plurality of data lines 7 are provided so as to correspond to the respective columns of the pixel electrodes 14.

In addition, thin-film transistors (hereinafter, simply referred to as "TFTs") 15 for forming the pixels are provided in the intersections between the scanning lines 8 and the data lines 7. A TFT 15 for each pixel is connected to a data line 7 and a pixel electrode 14

corresponding to the TFT 15. The ON/OFF states of the TFT 15 are controlled by a signal supplied through a scanning line 8 corresponding to the TFT 15.

On the entire surface of the substrate 12 of the liquid crystal panel 13, a common electrode 16 is formed. A pixel capacitance is formed in a portion in which the common electrode 16 on the substrate 12 faces the pixel electrodes 14 via the liquid crystal layer.

In addition, the scanning lines 8 are connected to a scanning driver 18 for sequentially driving the scanning lines 8 based on a timing signal supplied from a controller 19. On the other hand, the data lines 7 are connected to a data driver 17 for outputting a gray-scale display signal corresponding to video signal data to the data lines 7 based on the timing signal supplied from the controller 19.

The data driver 17 receives four reference gray-scale voltages V0, V2, V5 and V7 which are generated in a gray-scale voltage generator 20, so as to perform a gray-scale tone display at eight stages in response to the video signal data D0, D1 and D2 having 3 bits by way of the oscillating voltage method using these gray-scale reference voltages. Furthermore, a counter voltage generator 21 generates a counter voltage. The counter voltage is applied to the common electrode 16.

In order to prevent the deterioration of the liquid crystal, an alternating current drive for inverting the polarity of a voltage applied to the liquid crystal in the respective pixels at a predetermined

period by alternately switching the potential level of the gray-scale reference voltage and that of the counter voltage between high and low is performed. The switching of the voltage levels is performed in (synchronization) with a polarity switching signal POL supplied from the controller 19.

Figure 6 illustrates a 3-bit digital driver 200 included in the data driver 17. The digital data driver 17 includes a plurality of output circuits for outputting a data signal to data lines (or source lines) of the active-matrix type liquid crystal display device. The digital driver 200 is one of a plurality of output circuits included in the digital data driver 17. Thus, the digital driver 200 corresponds to one output from the digital data driver 17.

The digital driver (output circuit) 200 outputs a gray-scale display signal to the corresponding data line of the liquid crystal display device based on the video signal data D0, D1 and D2. The output circuit 200 includes: a sampling circuit 210 for sampling the video signal data D0, D1 and D2 based on a control signal TS; a storage memory 220 for storing the output of the sampling circuit 210 based on a control signal LP; and a selection control circuit 230 for selecting one of the gray-scale reference voltages V0, V2, V5 and V7 based on the data stored in the storage memory 220 so as to output a gray-scale display signal at a predetermined level to a data line.

As shown in Figure 7, the selection control circuit 230 includes: four analog switches ASW0, ASW2, ASW5

and ASW7 connected to a gray-scale reference power supply from which voltages having the levels of V0, V2, V5 and V7 are generated; and a selector 231 functioning as a digital circuit for selectively controlling the opened/closed states of the analog switches. The video signal data D0 to D2 stored in the storage memory 220 and a signal T3 having a duty ratio of 2:1 as shown in Figure 8 are supplied to the selector 231. The selector 231 selects a predetermined pair of the four analog switches based on the video signal data D0 to D2 so as to complementarily control the opened/closed states of the selected pair of analog switches in accordance with the timing of the signal T3. In this case, the gray-scale reference power supply is provided outside of an LSI constituting the driver 17.

Next, the operation of the digital driver will be described.

The logical structure of the selector 231, i.e., the relationship between input and output of the selector 231 is shown in following Logic Table 1.

[Table 1]

D2	D1	D0	S0	S2	S5	S7
0	0	0	1			
0	0	1	*t3	t3		
0	1	0		1		
0	1	1		t3	*t3	
1	0	0		*t3	t3	
1	0	1			1	
1	1	0			t3	*t3
1	1	1				1

In this table, D2, D1 and D0 are the 3-bit inputs to the selector 231 which are stored in the storage memory 220; and S0, S2, S5 and S7 are outputs from the selector 231 and function as control signals for the analog switches ASW0, ASW2, ASW5 and ASW7, respectively. Herein, when the signal T3 is at a high level, t3 is "1", and when the signal T3 is at a low level, t3 is "0". To the contrary, when the signal T3 is at a high level, *t3 is "0", and when the signal T3 is at a low level, *t3 is "1". The blanks in this table represent that the control signal is "0".

For example, when the video signal data is "1" (D2 = 0, D1 = 0, and D0 = 1), the control signal S0 has an inverted waveform of that of the signal T3 while the

control signal S2 has the same waveform as that of the signal T3. It is assumed that the respective analog switches ASW0, ASW2, ASW5 and ASW7 are turned on when the respective control signals S0, S2, S5 and S7 are high ("1"). In this case, the output OUT of the output circuit 200 has a waveform oscillating between the two gray-scale reference voltages V0 and V2 at a duty ratio of 2:1, as shown in Figure 9A.

By setting the period of the oscillating signal, i.e., the period of the signal T3, to be sufficiently shorter than the period of the cutoff frequency of the liquid crystal display device functioning as a low-pass filter, DC components represented as an average value of the oscillating voltage is supplied to the pixels.

Figures 9B, 9C and 9D show the waveforms output from the output circuit 200 when the video signal data is "3", "4" and "6", respectively. The following Table 2 shows the relationship between the video signal data input to this 3-bit driver and the output voltage of the driver.

[Table 2]

Video signal data				Output voltages
Decimal number	D2	D1	D0	V
0	0	0	0	V0
1	0	0	1	$\frac{V0+2xV2}{3}$
2	0	1	0	V2
3	0	1	1	$\frac{2xV2+V5}{3}$
4	1	0	0	$\frac{V2+2xV5}{3}$
5	1	0	1	V5
6	1	1	0	$\frac{2xV5+V7}{3}$
7	1	1	1	V7

The above-described method for driving a display device by an oscillating voltage method is disclosed in detail, for example, in Example 11 (columns 50 to 53) of Japanese Laid-Open Patent Publication No. 6-27900.

According to the above-described oscillating voltage method, it is possible to reduce considerably the number of gray-scale reference voltages to be externally applied. Therefore, this method is advantageous in that display can be performed at a far larger number of gray-scale tones than the number of the gray-scale power

supplies provided. However, this oscillating voltage method has drawbacks under certain conditions. Hereinafter, the drawbacks of this method will be described in detail.

Figure 10 shows the arrangement of the data lines on the liquid crystal panel 13. As shown in Figure 10, the data lines are divided into a plurality of sets, each of which consists of three lines corresponding to the three sub-pixels in red (R), green (G) and blue (B) constituting each one pixel, and the sets of data lines are sequentially arranged from one end of the liquid crystal panel 13 so as to be alternately disposed from the upper side of the panel and the lower side thereof. In Figure 10, an odd-numbered set of data lines corresponding to the three sub-pixels in R, G and B are denoted by S_{RU}, S_{GU} and S_{BU}, and the respective connection terminals of the data lines are extended from the upper end portion of the liquid crystal panel 13 so that these lines are driven by an upper-side driver disposed above the liquid crystal panel 13. On the other hand, an even-numbered set of data lines corresponding to the three sub-pixels in R, G and B are denoted by S_{RL}, S_{GL} and S_{BL}, and the respective connection terminals of the data lines are extended from the lower end portion of the liquid crystal panel 13 so that these lines are driven by a lower-side driver disposed below the liquid crystal panel 13. Therefore, the liquid crystal panel 13 shown in Figure 10 has a structure in which plural sets of data lines, each of which corresponds to a set of three sub-pixels, are alternately arranged on the upper side and on the lower side of the liquid crystal panel 13 so that the connection terminals thereof are alternately extended

upward and downward and that the sets of data lines are alternately driven by the upper-side and lower-side drivers disposed above and below the liquid crystal panel 13, respectively. Hereinafter, such a structure will be referred to as a "alternately extended comb-shaped drive structure", or simply referred to as a "comb-shaped structure".

Furthermore, a case where the liquid crystal panel having such a comb-shaped structure is driven by the 3-bit driver will be described below.

Figure 11 shows an upper-side driver 17a and a lower-side driver 17b together with the liquid crystal panel 13. In Figure 11, each set of three data lines corresponding to the three sub-pixels in R, G and B shown in Figure 10 is integrated into one data line S_U or S_L. In other words, the data line S_U includes a set of data lines S_{RU}, S_{GU} and S_{BU} having extended terminals from the upper end of the liquid crystal panel 13 while the data line S_L includes a set of data lines S_{RL}, S_{GL} and S_{BL} having extended terminals from the lower end of the liquid crystal panel 13.

In the following description, a set of three data lines corresponding to a set of three sub-pixels should be regarded to be one data line for illustrating a method for driving a liquid crystal panel. The reason is as follows. A color is originally displayed by using a set of three colors, i.e., red, green and blue. Accordingly, it is only because of the structure of the liquid crystal panel that the three colors are distributed among the three data lines, and therefore, a set of three data

lines corresponding to one pixel is regarded as one data line for simplicity.

Next, a pixel **UP1** closest to the upper-side driver **17a** and a pixel **UPL** farthest from the upper-side driver **17a** will be compared in the display device (or liquid crystal panel) driven by the upper-side driver **17a** and the lower-side driver **17b** as shown in Figure 11.

Figure 12 shows an equivalent circuit of the loads for the driver including the data lines. In Figure 12, **R1** and **C1** denote the resistance component and the capacitance component, respectively, existing between the output of the driver and the TFT of the pixel **UP1** as concentrated constants. The concentrated constants include an output resistance of the driver, the connection resistance in the terminal portion, the capacitance, and the like. The resistance and the capacitance of the data lines existing as distribution constants are denoted by r and c, respectively. In Figure 12, the TFT is simply shown as a switch, and the arrows of the respective capacitances indicate that all the capacitances are connected to the common electrode. These arrows indicate the same meanings in the following description.

As is apparent from Figure 12, resistances and capacitances of the data lines exist between the pixel **UP1** and the pixel **UPL**. Figure 13A shows an equivalent circuit of the loads involved to the pixel **UP1** relative to the output of the driver when the TFT for the pixel **UP1** is turned on, while Figure 13B shows an equivalent circuit of the loads involved to the pixel **UPL** relative to the output of the driver when the TFT for the

pixel UPL is turned on. In Figures 13A and 13B, RON denotes the ON resistance of the TFT, while RL and CL denote the concentrated constants of the resistance and the capacitance converted from the distribution constants r and c, respectively. As shown in Figures 13A and 13B, the related load of the pixel UP1 is different from that of the pixel UPL in the additional circuit section as indicated by the square in the broken line in Figure 13B. The additional circuit section provides the difference of the characteristics of a low pass-filter between the pixel UP1 and the pixel UPL.

Figure 14 shows the variations in the potential of the respective pixels which are driven by the driver in a case where the driver outputs an oscillating voltage corresponding to the video signal data of "3". In Figure 14, the variation in the waveform of the actual potential is exaggerated. In actuality, the variation level of the potential is far smaller as compared with the potential difference between the gray-scale reference voltages V2 and V5. The potential differences ΔUP1 and ΔUPL (Figure 14), indicating the deviations from an ideal target voltage V3, are set to be as small as 10 mV and 5 mV, respectively. Such variations in the potential of the respective pixels are generally negligible, since it is theoretically possible to reduce this deviation to any degree by increasing the frequency of the oscillating voltage. However, in a high-definition liquid crystal panel such as an "Extended Graphic Array" (XGA, trademark of IBM Corp.) and "Engineering Work Station" (EWS), in particular, the physical dimension of each pixel is smaller than that of the pixel in a conventional liquid crystal panel such as "Video Graphic Array" (VGA, trade-

mark of IBM Corp.), so that the capacitance in the pixel portion adversely decreases in proportion to the dimension of the pixel. In addition, in driving such a high-definition liquid crystal panel like a XGA or EWS panel, one output period of the driver is shorter than the period of a conventional VGA liquid crystal panel. Therefore, in order to sufficiently charge such a small pixel during the short period of time, the liquid crystal panel is frequently designed so that the ON resistance of the TFT becomes smaller as compared with a conventional VGA liquid crystal panel. Herein, the "one output period" refers to a period during which the TFT is turned on by the gate driver (or the scanning driver circuit) and the pixel is charged. The length of this output period is substantially equal to that of one horizontal period.

If the dimension of one pixel is small, then the resistance **RON** and the capacitance **CLC** are reduced in the equivalent circuit shown in Figure 13. In other words, the circuit cannot efficiently function as a low-pass filter any longer. Therefore, in the case of driving a high-definition liquid crystal panel like a XGA or EWS panel, it is necessary to set the frequency of the oscillating voltage to be higher as compared with the case of driving a conventional VGA display device (or liquid crystal panel) in order to obtain a deviation, i.e., the potential variation in the pixel, equal to that of the VGA device.

However, in a driver originally designed so as to drive a VGA type display device, it is difficult to set the oscillation frequency to be higher than a prescribed

value. This is because the output circuit of the driver is designed so as not to exceed an upper limit of the frequency of the oscillating voltage. The rising/falling characteristics of the analog switches of the output circuit are one of the factors to be carefully determined in designing the output circuit. In an oscillating voltage method, the variation in the rising/falling time of an analog switch varies the duty ratio of the oscillating voltage to be output. Therefore, if the frequency of the oscillating voltage is determined, then the permissible range of the variation in the rising/falling characteristics is naturally determined. This characteristic is varied because of various factors in the fabrication process. Accordingly, if this characteristic is excessively suppressed, then the quality of the elements constituting an analog switch is excessively deteriorated, so that the necessary cost becomes adversely increased.

Nevertheless, in actuality, there is no problem in increasing the operation frequency of an analog switch. This is because, an outputting analog switch fabricated by a C-MOS process has a sufficiently large margin in the operation frequency. For example, even in the case where a driver is designed while setting the frequency of the oscillating voltage to be 2 MHz, an analog switch can be easily operated at about 20 MHz. Therefore, if the frequency of the oscillating voltage is set to be higher than a prescribed value while maintaining the variation in the rising/falling time of the analog switch to be constant, then the influence of the variation in the rising/falling time on one period becomes relatively large.

Therefore, if the frequency of the oscillating voltage is set to be higher than the prescribed value, then the charge potential of the pixel is likely to be adversely varied because of the reasons other than the deterioration in the low-pass filter characteristics.

On the other hand, it is possible to re-design a driver so as to deal with a high oscillation frequency in the initial stage of the design. However, such a design requires much labor and cost. In addition, not only the driver thus designed tends to have an output circuit with a large area, but also the quality of the driver needs to be managed more strictly even during the fabrication process thereof, so that the cost is considerably increased.

Another serious problem is the increase in the consumed power caused by the increase in the frequency of the oscillating voltage. Since the consumed power is represented by fcV^2 (where f is frequency, c is load capacitance and V is voltage), the consumed power increases in proportion to the frequency. It is noted that the consumed power refers to the power consumed only in the circuit section for driving the loads, not the power consumed in the entire liquid crystal display device. The power consumed in the entire liquid crystal display device is different from the power consumed only in the section for driving the loads, and includes a lot of factors other than the frequency. As shown in Figure 15, even when the frequency of the oscillating voltage is 0, a certain amount of power W0 is consumed. The power consumption increases at a constant rate from the certain amount of power W0 in relation to the increase in the

frequency of the oscillating voltage.

Hereinafter, specific defects caused by the variation in the voltage applied to the pixel to be driven by the oscillating voltage method will be described.

In the foregoing description, the waveforms (of the voltages applied to the pixels) shown in Figure 14 are those of the upper-side driver. Naturally, those of the lower-side driver are the same as the waveforms shown in Figure 14. Therefore, as represented in parentheses in Figure 14, the voltage waveform for the pixel LPL closet to the lower-side driver correspond to the waveform for the pixel UP1, and the voltage waveform for the pixel LP1 farthest from the lower-side driver correspond to the waveform for the pixel UPL. In other words, the pixel closest to the upper-side driver and the pixel farthest from the upper-side driver have a voltage waveform opposite to that of the pixel closest to the lower-side driver and that of the pixel farthest from the lower-side driver, respectively.

It is to be noted that the pixel UP1 is adjacent to the pixel LP1 and that the pixel UPL is adjacent to the pixel LPL in this case. The difference in the waveforms of the horizontally adjacent pixels should be regarded as a serious problem.

Figure 16 shows the falling edge timing of the pulse output from the gate in addition to the waveforms shown in Figure 14. In this case, it is assumed that the circuit section has poor low-pass filter characteristics,

the variation range ΔUP1 (Figure 14) of the voltage applied to the pixel closest to the driver is 40 mV and the variation range ΔUPL (Figure 14) of the voltage applied to the pixel farthest from the driver is 20 mV.

Since the TFT is turned off by the falling edge of the gate signal, the pixel voltage at the falling edge is maintained during the OFF period and determines the transmission rate of the liquid crystal, or the gray-scale tones. Therefore, if the gate off timing is located at the point a of the waveform of the voltage applied to the pixel as shown in Figure 16, then the potential difference between the horizontally adjacent pixels becomes maximum (20 mV in this case). On the other hand, if the off timing is located at the point b, then the potential difference becomes minimum (0 in this case).

In the case of actually driving a liquid crystal panel by an oscillating voltage method, when the gate off timing happens to be located in the vicinity of the point a as described above, the gray-scale tones in the adjacent pixels become slightly different from each other. As a result, as shown in Figure 17, fine stripes 13a are adversely observed in the vicinities of the upper and lower end portions of the display panel 13. On the other hand, in the remaining portions of the display panel 13 excluding the upper and lower end portions thereof, the waveform of the voltage applied to the pixels is at an intermediate level between the levels of the two waveforms shown in Figure 14, so that the potential difference is small and the above-described defects are not observed.

In order to eliminate such defects, the inventors of the present invention have already developed the following method.

This method involves adjusting the gate off timing within one period of the oscillating voltage, and more specifically, adjusting a control signal for determining the off timing of the output switch in the gate driver within one period of the oscillating voltage.

According to this method, it is possible to avoid the turning off of the TFT in the vicinity of the point a shown in Figure 16. More advantageously, it is possible to set the off timing of the TFT in the vicinity of the point b shown in Figure 16. As a result, it is possible to eliminate the above-described defects, i.e., the fine stripes observable in the vicinities of the upper and lower end portions of the display device depending upon the gate off timing in the oscillating voltage method.

As described above, the method developed by the present inventors is very advantageous. However, depending upon various conditions, such as loads of the liquid crystal panel and the kind of driver, the above-described defects cannot be eliminated in some cases.

Hereinafter, the defects which cannot be eliminated by the method for adjusting the gate off timing during one period of the oscillating voltage will be described.

Figure 18 shows the output waveforms W1 and W2 of the oscillating voltages in two patterns output from the

3-bit driver (see Figures 6 to 9) mentioned above. In Figure 18, the abscissas indicate the time commonly applied to the two output waveforms W1 and W2, while the ordinates indicate the voltages independently drawn for the two output waveforms W1 and W2.

The output waveform W1 is the waveform of the gray-scale reference voltages V0 and V2 in a positive output time period, i.e., the period during which the pixels to be AC driven are charged at a positive potential, or the waveform of the gray-scale reference voltages V5 and V7 in a negative output time period, i.e., the period during which the pixels to be AC driven are charged at a negative potential. On the other hand, the output waveform W2 is the waveform of the gray-scale reference voltages V5 and V7 in a positive output time period, or the waveform of the gray-scale reference voltages V0 and V2 in a negative output time period.

As is apparent from Figure 18, the points a and b in which the deviation, i.e., the difference in the level of the applied voltage in one data between the pixel closest to the driver and the pixel farthest from the driver (hereinafter, referred to as a deviation in the voltage applied to the pixels), becomes maximum and minimum, respectively, are the same in both waveforms. Therefore, the off timing of the TFT is required to be located in the vicinity of the point b or the point b' of both the waveforms W1 and W2. Since the variation rate of the potential in the pixel in the vicinity of the point b is smaller as compared with the point b', a larger margin with respect to the deviation of the timing exists at the point b. Therefore, a better result is

likely to be obtained when the off timing is set at the point b.

In the case of using a driver having output waveforms of the oscillating voltage in which all the points having a minimum deviation are totally different from each other, the above-described defects cannot be eliminated by the above method developed by the present inventors.

Figure 19 shows the output waveforms W1 and W3 of the oscillating voltage of the 3-bit driver in which the deviation becomes minimum at different points. In Figure 19, the horizontal axis indicates time which is commonly used for the two output waveforms W1 and W3, while the vertical axis indicates the voltages independently drawn for the two output waveforms W1 and W3.

As shown in Figure 19, in the driver having such output waveforms W1 and W3, the deviation of the voltage applied to the pixels becomes minimum at the point b1 in the output waveform W1, while the deviation of the voltage applied to the pixels becomes maximum at the same point b1 in the output waveform W3. To the contrary, the deviation of the voltage applied to the pixels becomes minimum at the point b2 in the output waveform W3, while the deviation of the voltage applied to the pixels becomes maximum at the same point b2 in the output waveform W1.

Therefore, according to the above method developed by the present inventors, the points b1 and b2 in the waveforms of the oscillating voltage cannot be used

as the gate off timings. In this method, by setting the gate off timings at the points b1' and b2' in the waveforms of the oscillating voltage instead, satisfactory results can be obtained in practical use. This is because, at the point b1' in the output waveform W1 where the deviation of the voltage applied to the pixels becomes minimum, the deviation of the voltage applied to the pixels is at a rather low level in the output waveform W3. Similarly, at the point b2' in the output waveform W3 where the deviation of the voltage applied to the pixels becomes minimum, the deviation of the voltage applied to the pixels is at a rather low level in the output waveform W1.

Nevertheless, even if the gate off timings are set at such points, it is impossible to establish a complete accordance between the points of the two output waveforms W1 and W3 where the deviation of the voltage applied to the pixels becomes minimum. In addition, as described above, the potential variation rate of the oscillating voltage becomes large in the vicinities of these points b1' and b2', and therefore, the adjustment conditions become very strict.

SUMMARY OF THE INVENTION

The method of this invention is directed to a method for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plurality of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element.

The method includes the steps of: a) applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; b) applying a first scanning signal to a first scanning line, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal; and c) applying a second scanning signal to a second scanning line adjacent to the first scanning line, the second scanning signal defining a second timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second timing being different from the first timing.

In one embodiment of the present invention, the second pixel is adjacent to the first pixel in a longitudinal direction of the data lines.

In another embodiment of the present invention, the method further includes a step of alternately repeating the steps b) and c) for each of the plurality of scanning lines.

In still another embodiment of the present invention, each of the plurality of pixels includes a set of sub-pixels and each of the plurality of data lines includes a set of sub-data lines, each of the set of sub-data lines being connected to each of the set of sub-pixels.

Another method of this invention includes the steps of: a) applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; b) applying a first scanning signal to a first scanning line in a first frame, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal; and c) applying a second scanning signal to the first scanning line in a second frame different from the first frame, the second scanning signal defining a second timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second timing being different from the first timing.

In one embodiment of the present invention, the second frame is subsequent to the first frame.

In another embodiment of the present invention, the method further includes a step of alternately repeating the steps b) and c) for each frame.

In still another embodiment of the present invention, the method further includes a step of d) applying a third scanning signal to the first scanning line in a third frame different from the second frame, the third scanning signal defining a third timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the third

timing being different from the second timing.

In still another embodiment of the present invention, the method further includes a step of cyclicly repeating the steps b), c) and d) for each frame.

In still another embodiment of the present invention, further includes a step of e) applying a fourth scanning signal to a second scanning line adjacent to the first scanning line, the fourth scanning signal defining a fourth timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fourth timing being different from the first timing.

In still another embodiment of the present invention, the method further includes a step of alternately repeating the steps b) and e) for each of the plurality of scanning lines.

In still another embodiment of the present invention, the fourth timing in the step e) is substantially equal to the second timing in the step c).

In still another embodiment of the present invention, the method further includes a step of f) applying a fifth scanning signal to a third scanning line adjacent to the second scanning line, the fifth scanning signal defining a fifth timing at which a state of a third switching element connected to a third pixel adjacent to the second pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the

fifth timing being different from the first timing.

In still another embodiment of the present invention, the method further includes a step of cyclicly repeating the steps b), e) and f) for each of the plurality of scanning lines.

In still another embodiment of the present invention, the fourth timing in the step e) is substantially equal to the second timing in the step c) and wherein the fifth timing in the step f) is substantially equal to the third timing in the step d).

In still another embodiment of the present invention, each of the plurality of pixels includes a set of sub-pixels and each of the plurality of data lines includes a set of sub-data lines, each of the set of sub-data lines being connected to each of the set of sub-pixels.

In another aspect of the present invention, a driving circuit for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plurality of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element, the driving circuit includes: a data driver for applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; and a scanning driver for applying a first scanning signal to a first scanning line and a second scanning signal to a second scanning line adjacent to the first

scanning line, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second scanning signal defining a second timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, and the second timing being different from the first timing.

In one embodiment of the present invention, the second pixel is adjacent to the first pixel in a longitudinal direction of the data lines.

Another driving circuit for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plurality of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element, the driving circuit includes: a data driver for applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; and a scanning driver for applying a first scanning signal to a first scanning line in a first frame and a second scanning signal to the first scanning line in a second frame different from the first frame, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second scanning signal defining a second timing at which

the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, and the second timing being different from the first timing.

In one embodiment of the present invention, the second frame is subsequent to the first frame.

In another embodiment of the present invention, the scanning driver further applies a third scanning signal to the first scanning line in a third frame different from the second frame, the third scanning signal defining a third timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the third timing being different from the second timing.

In still another embodiment of the present invention, the scanning driver further applies a fourth scanning signal to a second scanning line adjacent to the first scanning line, the fourth scanning signal defining a fourth timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fourth timing being different from the first timing.

In still another embodiment of the present invention, the scanning driver further applies a fifth scanning signal to a third scanning line adjacent to the second scanning line, the fifth scanning signal defining a fifth timing at which a state of a third switching

element connected to a third pixel adjacent to the second pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fifth timing being different from the first timing.

According to the present invention, the relative positions of the off timings of a switching element constituting a pixel, which are selected with respect to the phase of the oscillating voltage output to the data lines, are set at different locations between adjacent pixels or close pixels. Accordingly, even when the variation width of the voltage applied to the pixel becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to adjacent pixels or close pixels can be averaged. Therefore, a defective display on the liquid crystal panel, caused by the difference in the variation widths of the voltage applied to the pixels, becomes less recognizable to the human eye. As a result, it is possible to prevent the stripes, caused by unsatisfactory low-pass filter characteristics of a liquid crystal panel driven by an oscillating voltage method, from being recognized on a part of the screen without increasing the frequency of the oscillating voltage.

According to the present invention, the relative positions of the off timings of a switching element, which are selected with respect to the phase of the oscillating voltage, are set at different locations between the pixels which are adjacent or close to each other along the longitudinal direction of the data lines. Accordingly, even when the variation width of the voltage

applied to the pixel becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to the pixels which are adjacent or close to each other along the longitudinal direction of the display screen can be averaged.

According to the present invention, the relative positions of the off timings of a switching element, which are different among the pixels and selected with respect to the phase of the oscillating voltage, are set at two locations different from each other with respect to the phase of the oscillating voltage. As a result, it is possible to prevent the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method while using a simplified circuit structure.

According to the present invention, the falling edge timings of the pulse output from a scanning driver for controlling the opened/closed states of a switching element by outputting a scanning signal to the switching element are varied so that the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage are different among the pixels. As a result, it is possible to realize a scanning driver for preventing the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method. Alternatively, the rising edge timings may be varied so that the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage are different among the pixels.

According to the present invention, the relative positions of the off timings of a switching element constituting a pixel, which are selected with respect to the phase of the oscillating voltage output to the data lines, are set at different locations between predetermined frames. Accordingly, even when the variation width of the voltage applied to the pixel becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to the pixels can be averaged between the predetermined frames. Therefore, a defective display on the liquid crystal panel, caused by the difference in the variation widths of the voltage applied to the pixels, becomes less recognizable to the human eye. As a result, it is possible to prevent the stripes, caused by unsatisfactory low-pass filter characteristics of a liquid crystal panel driven by an oscillating voltage method, from being recognized on a part of the screen without increasing the frequency of the oscillating voltage.

According to the present invention, the relative positions of the off timings of a switching element, which are selected with respect to the phase of the oscillating voltage, are set at different locations between the frames which are adjacent or close to each other. Accordingly, even when the variation width of the voltage applied to the pixel becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to the pixels can be averaged among the frames which are adjacent or close to each other.

In a method for driving a display device accord-

ing to the present invention, the relative positions of the off timings of a switching element, which are different among the frames and selected with respect to the phase of the oscillating voltage, are set at two locations different from each other with respect to the phase of the oscillating voltage. As a result, it is possible to prevent the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method while using a simplified circuit structure.

In a circuit for driving a display device according to the present invention, the falling edge timings of the pulse output from a scanning driver for controlling the opened/closed states of a switching element by outputting a scanning signal to the switching element are varied so that the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage are different among the frames. As a result, it is possible to realize a scanning driver for preventing the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method. Alternatively, the rising edge timings may be varied so that the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage are different among the pixels.

Thus, the invention described herein makes possible the advantage of providing a method and circuit for driving a display device in which it is possible to prevent the stripes, caused by unsatisfactory low-pass filter characteristics of a liquid crystal panel driven by an oscillating voltage method, from being recognized on a part of the screen without increasing the frequency

of the oscillating voltage.

This and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram showing the configuration of a circuit for changing the gate off timings at a period of two frames, which is included in a scanning driver of a driving circuit for a display device according to a first example of the present invention.

Figure 2A is a chart showing the waveform of the horizontal synchronization signal Hsync;

Figure 2B is a chart showing the waveform of the gate clock GCK' output from the circuit shown in Figure 1; and

Figure 2C is a chart showing rising edges of the gate clock GCK'.

Figure 3 is a diagram showing the configuration of a circuit for changing the gate off timings at a period of two lines and two frames, which is included in a scanning driver of a driving circuit for a display device according to a second example of the present invention.

Figure 4A is a chart showing the waveform of the horizontal synchronization signal Hsync;

Figure 4B is a chart showing the waveforms of the gate clock GCK' output from the circuit shown in Figure 3; and

Figure 4C is a chart showing rising edges of the gate clock GCK'.

Figure 5 is a waveform chart showing the oscillating voltage patterns of a 4-bit driver to which the present invention is applicable.

Figure 6 is a block diagram showing one of a plurality of output circuits constituting a 3-bit driver by utilizing an oscillating voltage method for a conventional active-matrix type liquid crystal display device.

Figure 7 is a diagram showing a detailed configuration of a selection controller in a conventional driver.

Figure 8 is a chart showing a waveform of a pulse signal having a duty ratio of 2:1 to be used for producing an oscillating voltage in an output circuit for a 3-bit driver according to the present invention and an output circuit for a conventional 3-bit driver.

Figures 9A to 9D are charts showing the waveforms of the oscillating voltages when the video signal data output from the output circuit of the 3-bit driver according to the present invention and that of the

conventional 3-bit driver are "1", "3", "4" and "6", respectively.

Figure 10 is a view schematically showing a configuration for a TFT liquid crystal panel constituting a conventional active-matrix type liquid crystal display device.

Figure 11 is a view showing an arrangement of the TFT liquid crystal panel, an upper-side driver and a lower-side driver disposed above and below the panel, as well as the configuration of the panel.

Figure 12 is a diagram showing an equivalent circuit of the TFT liquid crystal panel connected with a driver by using distribution constants.

Figures 13A and 13B are diagrams showing an equivalent circuit shown by concentrated constants which is converted from the equivalent circuit shown in Figure 12 by distribution constants.

Figure 14 is a chart showing the waveforms of the voltages applied to predetermined pixels when the video signal data is "3", or the waveform of the voltage applied to the pixel UP1 which is driven by the upper-side driver and is closest to the driver (or the pixel LPL which is driven by the lower-side driver and is closest to the driver) and the waveform of the voltage applied to the pixel UPL which is driven by the upper-side driver and is farthest from the driver (or the pixel LP1 which is driven by the lower-side driver and is farthest from the driver).

Figure 15 is a graph showing the relationship between a frequency of the oscillating voltage and a power consumption in a liquid crystal display device using the oscillating voltage method.

Figure 16 is a graph showing the positional relationship among the waveforms of the voltages applied to the pixel UP1 (or LPL) and the pixel UPL (or LP1) shown in Figure 14, and the falling timing of the gate pulse applied to the gate of the TFT.

Figure 17 is a view showing the fine stripes generated on the screen of the liquid crystal panel in a liquid crystal display device.

Figure 18 is a chart showing the waveforms of the oscillating voltages output from a 3-bit driver and the variations of the oscillating voltages at the respective pixels.

Figure 19 is a chart showing the waveforms of the oscillating voltages, different from those shown in Figure 18, output from a 3-bit driver and the variations of the oscillating voltages at the respective pixels.

Figure 20 is a diagram schematically showing the charge potentials of a pixel driven by a 3-bit driver in the respective frames.

Figure 21 is a diagram schematically showing the charge potentials of a pixel driven by a 3-bit driver in the respective frames and lines.

Figure 22 is a diagram showing an entire configuration for an exemplary liquid crystal display device of the present invention and a conventional liquid crystal display device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First, the fundamental principles of the present invention will be described.

Again, Figure 19 shows the waveforms W1 and W3 of oscillating voltage signals output from the data driver 17 to the data lines 7. The oscillating voltage signals applied to the data lines 7 oscillate in an oscillating period T. The oscillating voltage signal having waveform W1 is a data signal applied to the corresponding data line during a positive output period in a case where the video signal data is "1" as shown in Table 2. The oscillating voltage signal having waveform W3 is a data signal applied to the corresponding data line during a negative output period in a case where the video signal data is "1" as shown in Table 2.

The waveforms of voltage signals for charging the corresponding pixel based on the oscillating voltage signals are indicated by w1 and w3. Herein, the desired DC voltages to be applied to the corresponding pixel are indicated by V1DC and V2DC.

It is assumed that the deviation from the desired DC voltage V1DC at the point a1 is denoted by $+\Delta a1$, while the deviation from the desired DC voltage V1DC at the point a1' is denoted by $-\Delta a1$.

According to the driving method of the present invention, the off gate timings are different from each other in different frames. For example, the off gate timings are repeatedly changed in three successive frames (referred to as frame 1, frame 2 and frame 3, respectively). More specifically, the off gate timing is a timing at the point **a1** in frame 1; the off gate timing is a timing at the point **b1** in frame 2; and the off gate timing is a timing at the point **a1'** in frame 3, for example (see, Figure 19). In the present specification, "the off gate timing" is defined as a timing at which a state of a switching element connected to the corresponding pixel is changed from ON to OFF in one oscillating period **T** of the oscillating voltage signal output to the data lines.

Here, it is assumed that an arbitrary pixel is fixed as a specified pixel. Figure 20 shows the voltages which are charged to the specified pixel in the successive frames. Specifically, the scanning driver 18 (Figure 22) applies a scanning signal which defines a gate off timing of the point **a1** to the corresponding scanning line 8, so as to apply a voltage **V1DC+Δa1** to the specified pixel in frame 1; the scanning driver 18 applies a scanning signal which defines a gate off timing of the point **b1** to the corresponding scanning line 8, so as to apply a voltage **V1DC** to the specified pixel in frame 2; and the scanning driver 18 applies a scanning signal which defines a gate off timing of the point **a1'** to the corresponding scanning line 8, so as to apply a voltage **V1DC-Δa1** to the specified pixel in frame 2. Such applications of the voltages to the specified pixel are cyclicly repeated in three successive frames.

Herein, the deviations +Δal and -Δal are very small, so that the difference in the transmission rates of the liquid crystal can hardly be recognized visually. As a result, substantially no visual defects or secondary effects such as flickering are caused, and the transmission rates of the liquid crystal are averaged among the respective frames, so that only the transmission rate corresponding to the desired DC voltage V1DC can be visually recognized.

Similarly, with respect to the oscillating voltage signal having waveform W3 shown in Figure 19, the transmission rates of the liquid crystal are averaged among the respective frames, so that only the transmission rate corresponding to the desired DC voltage V2DC can be visually recognized. Thus, a highly uniform quality is realized over the entire screen with respect to both the output patterns W1 and W3 shown in Figure 19.

The present invention is applicable not only to a cyclic change of the gate off timings in the respective frames, but also to a cyclic change of the gate off timings by every three successive scanning lines in the order of the point a1, the point b1 and the point a1'.

Figure 21 schematically shows the voltages applied to the three specified pixels adjacent to each other in the longitudinal direction of data lines 7. In this case, in each pixel, the relationship among the respective frames is the same as that of the previous example shown in Figure 20. In addition, the off gate timings are repeatedly changed in three successive scanning lines (denoted by line 1, line 2 and line 3,

respectively) in one frame.

Specifically, the scanning driver 18 applies a scanning signal which defines a gate off timing of the point a1 to the corresponding scanning line 8 (i.e., line 1), so as to apply a voltage V1DC+Δa1 to a first specified pixel in frame 1; the scanning driver 18 applies a scanning signal which defines a gate off timing of the point b1 to the corresponding scanning line 8 (i.e., line 2 adjacent to line 1), so as to apply a voltage V1DC to a second specified pixel adjacent to the first specified pixel in frame 1; and the scanning driver 18 applies a scanning signal which defines a gate off timing of the point a1' to the corresponding scanning line 8 (i.e., line 3 adjacent to line 2), so as to apply a voltage V1DC-Δa1 to a third specified pixel adjacent to the second specified pixel in frame 1. Such applications of the voltages to the specified pixel are cyclicly repeated in three successive scanning lines in one frame.

As a result, among the pixels which are vertically or horizontally adjacent to each other within one frame, the transmission rates of the liquid crystal are also averaged.

In the foregoing description, the polarity of the voltage applied to the pixel electrode and that of the voltage applied to the common electrode in the respective frames has not been mentioned in comparison for simplification. In general, with respect to a specified pixel, the polarity of the potential is inverted with respect to the common electrode in the respective frames. Therefore, strictly speaking, the potential applied to the

pixels shown in Figures 20 and 21 should be regarded as absolute values.

Hereinafter, the present invention will be described by way of illustrative examples with reference to the accompanying drawings.

The change of the relative positions of the off timings of the TFT with respect to the phase of the oscillating voltage output to the corresponding data line is realized by changing of the gate off timings with respect to the horizontal synchronization signal, in a case where an oscillating voltage is always output to a corresponding data line at an identical phase with respect to a horizontal synchronization signal. Also, the change of the gate off timings is realized by changing a timing of a rising edge of the gate clock without changing a timing of a falling edge of the gate clock, in a case where the scanning driver 18 (or the gate driver 18) is a type of a gate driver which turns on the gate at the falling edge of the gate clock and turns off the gate at the rising edge of the gate clock.

Example 1

Figure 1 shows the configuration of a circuit 101 for changing the gate off timings of the TFT in the respective scanning lines. The circuit 101 is included in the scanning driver 18 shown in Figure 22. In this example, the configuration of the active-matrix type liquid crystal display device including the circuit 101 shown in Figure 1 is the same as that of a device shown in Figure 22 except for the different scanning driver 18.

The circuit **101** is a timing controller for controlling the gate off timings of the TFT corresponding to a pixel in the respective scanning lines so as to generate a gate pulse signal having a particular pulse width. The timing controller **101** includes: a 1/2 T delay circuit **111** for receiving a gate clock **GCK** and delaying the gate clock **GCK** by the amount of time corresponding to one half of the period **T** of the oscillating voltage in response to the clock **CK**; an AND gate **112** to which the gate clock delayed by the delay circuit **111** and the gate clock **GCK** are input; and a 2 selector **113** for receiving the output of the AND gate **112** at a second input **B** and the gate clock **GCK** at a first input **A** and switching these two signals in response to a select signal. A control input **S** of the 2 selector **113** is connected to the output of a 2 divider **114** which divides a horizontal synchronization signal **Hsync** into two. In this case, when the input signal to the control input **S** is "0", the 2 selector **113** outputs a signal input through the first input **A** to the output Y. On the other hand, when the input signal to the control input **S** is "1", the 2 selector **113** outputs a signal input through the second input **B** to the output Y.

The 2 divider **114** is reset by a vertical synchronization signal **Vsync**, so that the gate off timings for the respective scanning lines become the same in all the frames.

As described above, the timing controller **101** alternately and repeatedly outputs a scanning signal having two kinds of gate off timings which are delayed by one-half of the period **T** of the oscillating voltage to

the respective scanning lines.

If the uppermost line of a liquid crystal panel is counted as a first line, then the gate off timing on an odd-numbered line is an ordinary off timing and the gate off timing on an even-numbered line is delayed from the off timing on the odd-numbered line by one-half of the period T of the oscillating voltage. As a result, the brightness of two vertically adjacent lines is visually averaged on the liquid crystal panel.

As described above, two kinds of off timings are used. This is because the deviations of the voltages applied to the pixel are averaged by providing an arbitrary off timing and another off timing which is delayed from the former off timing by one-half of the period T of the oscillating voltage, even in a case where an oscillating voltage having a duty ratio of 2:1 (Figure 19) is used. As a result, the level of the brightness on the liquid crystal panel is averaged. Thus, satisfactory effects can be obtained in practical use, and the circuit configuration can be advantageously simplified. In a case where an oscillating voltage having a duty ratio of 1:1 is used, the level of the brightness on the liquid crystal panel is averaged so as to completely correspond to a desired DC level.

Furthermore, the off timings may be changed in respective frames as well as in respective lines. In this case, a problem of flicker can also be advantageously solved.

Next, the operation of the scanning driver will

be described. The scanning driver 18 is also referred to as a gate driver 18.

In this example, it is assumed that a gate driver 18 turns on the gate at a falling edge of the gate clock GCK' and turns off the gate at a rising edge of the gate clock GCK'. The gate clock GCK to be used as a reference is delayed by the delay circuit 111 by one-half of the period T of the oscillating voltage, and the delayed signal and the original gate clock GCK used as the reference are input to the AND gate 112. Then, a signal in which only the rising edge of the gate clock GCK is delayed by one-half of the period T of the oscillating voltage is output from the AND gate 112.

Thereafter, the original gate clock GCK used as the reference and the gate clock having a rising edge which is delayed by one-half of the period T of the oscillating voltage, are input to the 2 selector 113. The two signals are alternately switched and output from the 2 selector 113 in response to a select signal. In this example, since a signal obtained by dividing the horizontal synchronization signal Hsync into two is used as the select signal to the 2 selector 113, gate clocks GCK' having different gate off timings among the respective lines are output through the output of the 2 selector 113.

Figure 2A shows the waveform of the horizontal synchronization signal Hsync. Figure 2B shows the waveform of the gate clock GCK' output from the 2 selector 113 of the timing controller 101. Figure 2C shows rising edges of the gate clock GCK'. As shown in Fig-

ure 2C, the gate off timings (i.e., the timings of the rising edges of the gate clock GCK') are different from each other among different horizontal periods. This means that the gate off timings are different from each other among the respective scanning lines.

As described above, since the off timings of the gate (switching element connected to the corresponding scanning line) are alternately changed in the respective scanning lines in this example, the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage become different among the pixels adjacent to each other in a vertical direction of the liquid crystal panel. Accordingly, even when the variation width of the voltage applied to the pixels becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to the pixels adjacent to each other in the vertical direction of the display screen of the liquid crystal panel can be averaged. Therefore, a defective display on the liquid crystal panel, caused by the difference in the variation widths of the voltage applied to the pixels, becomes less recognizable to the human eye. As a result, it is possible to eliminate such a defective display without increasing the frequency of the oscillating voltage when the liquid crystal panel is driven by an oscillating voltage method and the low-pass filter characteristics of the source lines are unsatisfactory.

In addition, a defective display caused by the variation of the low-pass filter characteristics in the respective panels can be eliminated to a large degree.

Furthermore, in this example, the relative positions of the off timings of a switching element, which are different among the pixels and selected with respect to the phase of the oscillating voltage, are set at two locations different from each other with respect to the phase of the oscillating voltage. As a result, it is possible to prevent the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method while using a simplified circuit structure.

Example 2

Figure 3 shows the configuration of a circuit 102 for changing the gate off timings of the TFT in the respective scanning lines and the respective frames. The circuit 102 is included in the scanning driver 18 shown in Figure 22. In this example, the configuration of the active-matrix type liquid crystal display device including the circuit 102 shown in Figure 3 is the same as that of a device shown in Figure 22 except for the scanning driver 18.

The circuit 102 is a timing controller for controlling the gate off timings of the TFT corresponding to a pixel in the respective scanning lines and the respective frames. That is to say, the circuit 102 not only changes the off timings of the respective lines in one frame, but also inverses the off timings of the respective lines in the next frame. As a result, the off timings can be averaged not only on the adjacent lines but also on one and the same line, so that the image can be visually averaged more effectively.

More specifically, in addition to the respective components of the timing controller **101** of the first example, the timing controller **102** further includes a second 2 divider **115** for dividing a vertical synchronization signal **Vsync** into two, and an exclusive-OR (XOR) circuit **116** to which the output of the second 2 divider **115** and the output of the 2 divider **114** for the horizontal synchronization signal **Hsync** are input. The output of the XOR circuit **116** is connected to the control input **S** of the 2 selector **113**. Except for the above-described points, the configuration of the timing controller **102** is the same as the configuration of the timing controller **101** of the first example shown in Figure **1**.

Next, the operation of the driver will be described.

In this example, since the vertical synchronization signal **Vsync** is input to the terminal **RESET** of the 2 divider **114**, the levels of the signals obtained by dividing the horizontal synchronization signal **Hsync** into two alternately become "0" and "1" in the respective frames, i.e., 0, 1, 0, 1, 0, 1, ... An exclusive-OR between this signal and the signals obtained by dividing the vertical synchronization signal **Vsync** into two is calculated by the exclusive-OR (XOR) circuit **116**. Accordingly, the levels of the signals obtained by dividing the horizontal synchronization signal **Hsync** into two alternately become "1" and "0" in the next frame, i.e., 1, 0, 1, 0, 1, 0, ... As a result, a driver for changing the gate off timings on the adjacent lines and in the adjacent frames on one and the same line is realized.

Figure 4A shows the waveform of the horizontal synchronization signal Hsync, Figure 4B shows the waveforms of the gate clock GCK' output from the 2 selector 113 of the timing controller 102, and Figure 4C shows rising edges of the gate clock GCK'. As shown in Figure 4C, the gate off timings (i.e., the timings of the rising edges of the gate clock GCK') are different in the respective scanning lines and the respective frames.

As described above, since the off timings of the gate (switching element connected to the corresponding scanning line) are alternately changed in the respective scanning lines and the respective frames in this example, the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage become different among the pixels adjacent to each other along the vertical direction of the liquid crystal panel and the pixels adjacent to each other along the horizontal direction thereof. Accordingly, even when the variation width of the voltage applied to the pixels becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to the pixels adjacent to each other along the vertical and horizontal directions on the display screen of the liquid crystal panel can be averaged. Therefore, a defective display on the liquid crystal panel, caused by the difference in the variation widths of the voltage applied to the pixels, becomes less recognizable to the human eye. As a result, it is possible to eliminate such a defective display without increasing the frequency of the oscillating voltage when the liquid crystal panel is driven by an oscillating voltage method and the low-pass filter characteristics of

the source lines are unsatisfactory.

The present invention is particularly applicable to a display device using a driver having an even larger number of oscillating voltage patterns, e.g., a 4-bit driver. Figure 5 shows the oscillating voltage patterns of a 4-bit driver. As shown in Figure 5, when a driver has a large number of oscillating voltage patterns as output waveforms, these patterns can be roughly classified into two types, i.e., the patterns in which the oscillation is switched in the first half of the period, and the patterns in which the oscillation is switched in the second half of the period. In this case, when the off timing of the TFT exists in the second half of the pattern in which the oscillation is switched in the first half of the period, the deviation at the switching point becomes large. On the other hand, in the pattern in which the oscillation is switched in the second half of the period, the deviation becomes small. Therefore, if the off timing of the TFT is fixed, the above-described defect is sometimes observed depending upon the conditions. Therefore, by changing the off timing of the TFT at two points which are located at appropriate positions in the first and second halves of the oscillating voltage, respectively, such a defect can be eliminated.

Naturally, the present invention is also effectively applicable to an 8-bit driver and the like.

As is apparent from the foregoing description, in the method for driving a display device according to present invention, the relative positions of the off timings of a switching element constituting a pixel,

which are selected with respect to the phase of the oscillating voltage output to the data lines, are set at different locations between adjacent pixels or close pixels. Accordingly, even when the variation width of the voltage applied to the pixels becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to adjacent pixels or close pixels can be averaged. Therefore, a defective display on the liquid crystal panel, caused by the difference in the variation widths of the voltage applied to the pixels, becomes less recognizable to the human eye. As a result, it is possible to prevent the stripes, caused by unsatisfactory low-pass filter characteristics of a liquid crystal panel driven by an oscillating voltage method, from being recognized on a part of the screen without increasing the frequency of the oscillating voltage.

In the method for driving a display device according to present invention, the relative positions of the off timings of a switching element constituting a pixel, which are selected with respect to the phase of the oscillating voltage output to the data lines, are set at different locations between predetermined frames. Accordingly, even when the variation width of the voltage applied to the pixels becomes different depending upon the distance from the pixel to the driver, the difference in the variation widths of the voltage applied to the pixels can be averaged between the predetermined frames. Therefore, a defective display on the liquid crystal panel, caused by the difference in the variation widths of the voltage applied to the pixels, becomes less recognizable to the human eye. As a result, it is possi-

ble to prevent the stripes, caused by unsatisfactory low-pass filter characteristics of a liquid crystal panel driven by an oscillating voltage method, from being recognized on a part of the screen without increasing the frequency of the oscillating voltage.

In the method for driving a display device according to the present invention, the relative positions of the off timings of a switching element, which are different among the predetermined pixels or frames and selected with respect to the phase of the oscillating voltage, are set at two locations different from each other with respect to the phase of the oscillating voltage. As a result, it is possible to prevent the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method while using a simplified circuit structure.

In a circuit for driving a display device according to the present invention, the falling timings of the pulse output from a scanning driver for controlling the opened/closed states of a switching element by outputting a scanning signal to the switching element are varied so that the relative positions of the off timings of the switching element with respect to the phase of the oscillating voltage are different among the predetermined pixels or frames. As a result, it is possible to realize a scanning driver for preventing the stripes from being recognized on a part of the liquid crystal panel driven by an oscillating voltage method.

Various other modifications will be apparent to and can be readily made by those skilled in the art

without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

What is claimed is:

1. A method for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plurality of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element,

the method comprising the steps of:

a) applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged;

b) applying a first scanning signal to a first scanning line, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal; and

c) applying a second scanning signal to a second scanning line adjacent to the first scanning line, the second scanning signal defining a second timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second timing being different from the first timing.

2. A method according to claim 1, wherein the second pixel is adjacent to the first pixel in a longitudinal direction of the data lines.

3. A method according to claim 1, further comprising a step of alternately repeating the steps b) and c) for

each of the plurality of scanning lines.

4. A method according to claim 1, wherein each of the plurality of pixels comprises a set of sub-pixels and wherein each of the plurality of data lines comprises a set of sub-data lines, each of the set of sub-data lines being connected to each of the set of sub-pixels.

5. A method for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plurality of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element,

the method comprising the steps of:

a) applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged;

b) applying a first scanning signal to a first scanning line in a first frame, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal; and

c) applying a second scanning signal to the first scanning line in a second frame different from the first frame, the second scanning signal defining a second timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second timing being different from the first timing.

6. A method according to claim 5, wherein the second

frame is subsequent to the first frame.

7. A method according to claim 5, further comprising a step of alternately repeating the steps b) and c) for each frame.

8. A method according to claim 5, further comprising

d) a step of applying a third scanning signal to the first scanning line in a third frame different from the second frame, the third scanning signal defining a third timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the third timing being different from the second timing.

9. A method according to claim 8, further comprising a step of cyclicly repeating the steps b), c) and d) for each frame.

10. A method according to claim 5, further comprising

e) a step of applying a fourth scanning signal to a second scanning line adjacent to the first scanning line, the fourth scanning signal defining a fourth timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fourth timing being different from the first timing.

11. A method according to claim 10, further comprising a step of alternately repeating the steps b) and e) for each of the plurality of scanning lines.

12. A method according to claim 10, wherein the fourth timing in the step e) is substantially equal to the second timing in the step c).

13. A method according to claim 10, further comprising

f) a step of applying a fifth scanning signal to a third scanning line adjacent to the second scanning line, the fifth scanning signal defining a fifth timing at which a state of a third switching element connected to a third pixel adjacent to the second pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fifth timing being different from the first timing.

14. A method according to claim 13, further comprising a step of cyclicly repeating the steps b), e) and f) for each of the plurality of scanning lines.

15. A method according to claim 13, wherein the fourth timing in the step e) is substantially equal to the second timing in the step c) and wherein the fifth timing in the step f) is substantially equal to the third timing in the step d).

16. A method according to claim 5, wherein each of the plurality of pixels comprises a set of sub-pixels and wherein each of the plurality of data lines comprises a set of sub-data lines, each of the set of sub-data lines being connected to each of the set of sub-pixels.

17. A driving circuit for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plural-

ity of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element,

the driving circuit comprising:

a data driver for applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; and

a scanning driver for applying a first scanning signal to a first scanning line and a second scanning signal to a second scanning line adjacent to the first scanning line, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second scanning signal defining a second timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, and the second timing being different from the first timing.

18. A driving circuit according to claim 17, wherein the second pixel is adjacent to the first pixel in a longitudinal direction of the data lines.

19. A driving circuit for driving a display device including a plurality of pixels; a plurality of scanning lines; and a plurality of data lines, each of the plurality of pixels being connected to one of the plurality of scanning lines and one of the plurality of data lines via a switching element,

the driving circuit comprising:

a data driver for applying an oscillating voltage signal to the data lines, the oscillating voltage periodically oscillating in a period during which a first pixel is charged; and

a scanning driver for applying a first scanning signal to a first scanning line in a first frame and a second scanning signal to the first scanning line in a second frame different from the first frame, the first scanning signal defining a first timing at which a state of a first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the second scanning signal defining a second timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, and the second timing being different from the first timing.

20. A driving circuit according to claim 19, wherein the second frame is subsequent to the first frame.

21. A driving circuit according to claim 19, wherein the scanning driver further applies a third scanning signal to the first scanning line in a third frame different from the second frame, the third scanning signal defining a third timing at which the state of the first switching element connected to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the third timing being different from the second timing.

22. A driving circuit according to claim 19, wherein the scanning driver further applies a fourth scanning signal

to a second scanning line adjacent to the first scanning line, the fourth scanning signal defining a fourth timing at which a state of a second switching element connected to a second pixel adjacent to the first pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fourth timing being different from the first timing.

23. A driving circuit according to claim 22, wherein the scanning driver further applies a fifth scanning signal to a third scanning line adjacent to the second scanning line, the fifth scanning signal defining a fifth timing at which a state of a third switching element connected to a third pixel adjacent to the second pixel is changed from ON to OFF in one oscillating period of the oscillating voltage signal, the fifth timing being different from the first timing.

FIG. 1

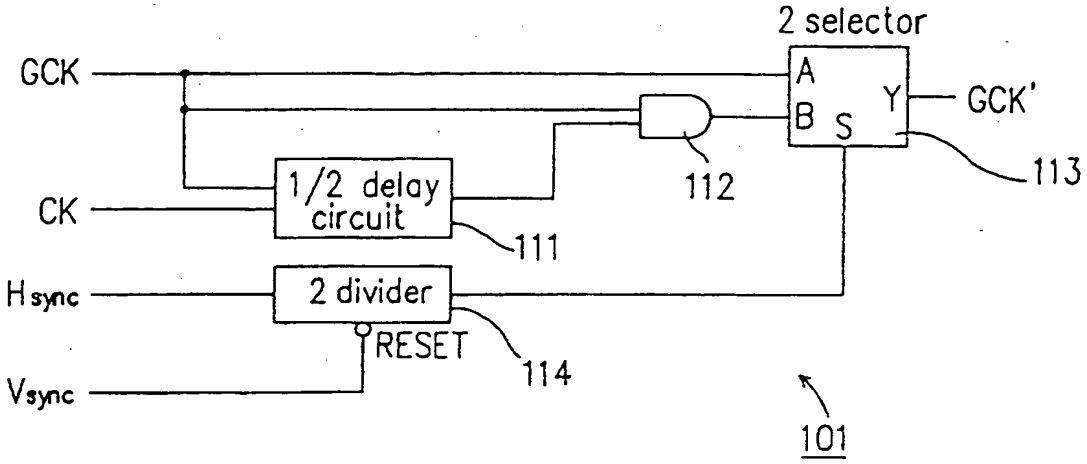


FIG. 2A

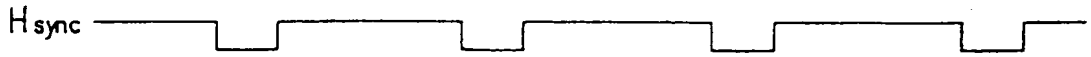


FIG. 2B

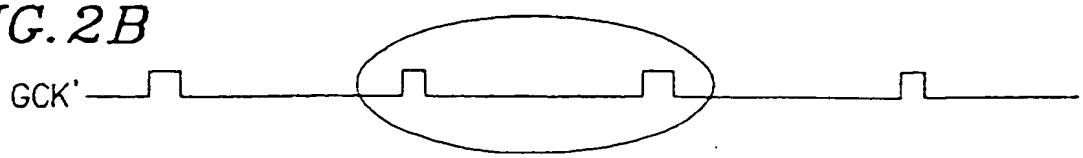


FIG. 2C

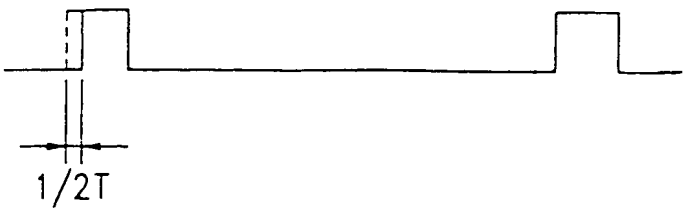


FIG. 3

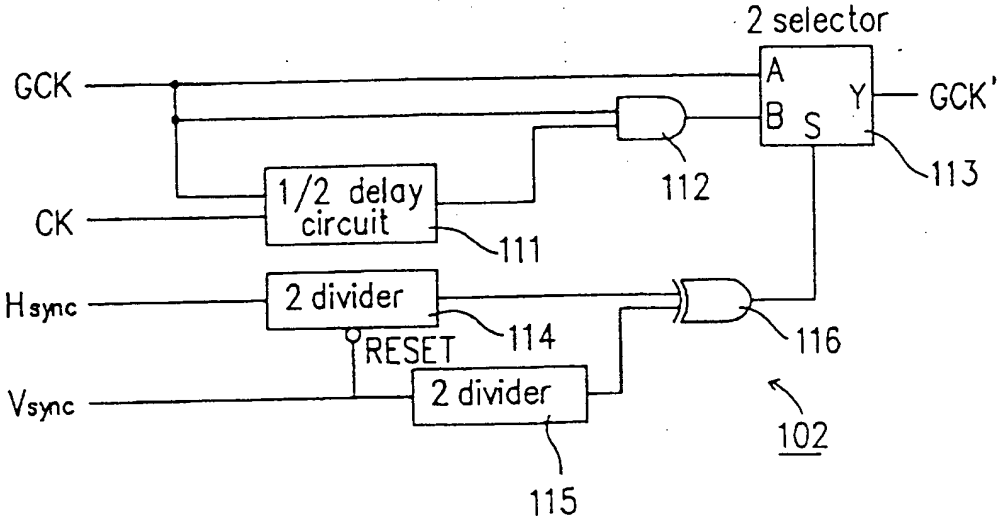


FIG. 4A

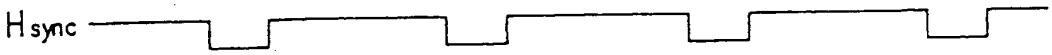


FIG. 4B

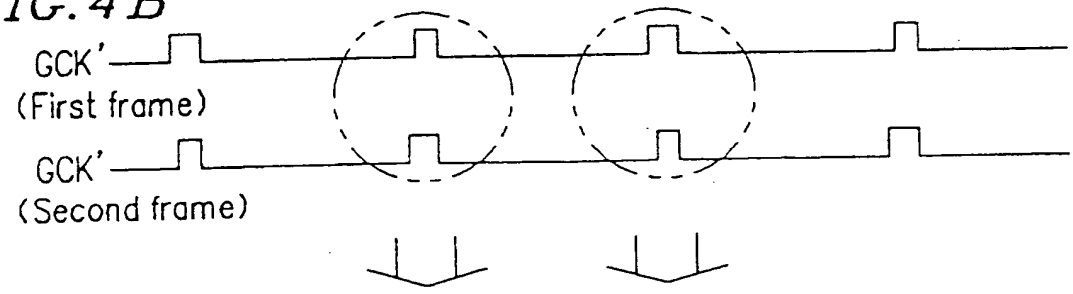


FIG. 4C

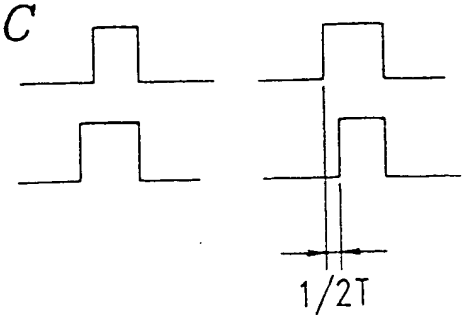


FIG.5

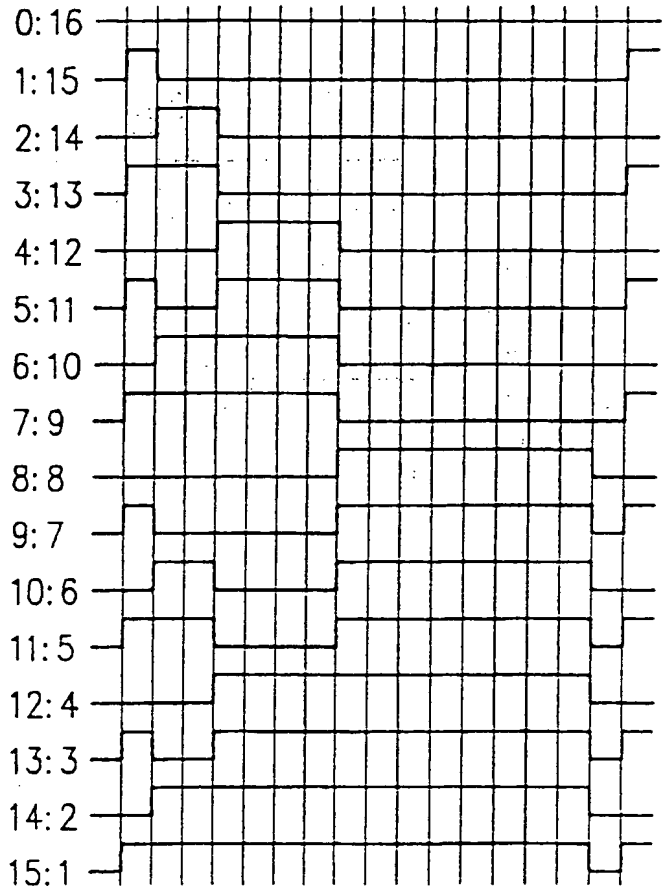


FIG.6 PRIOR ART

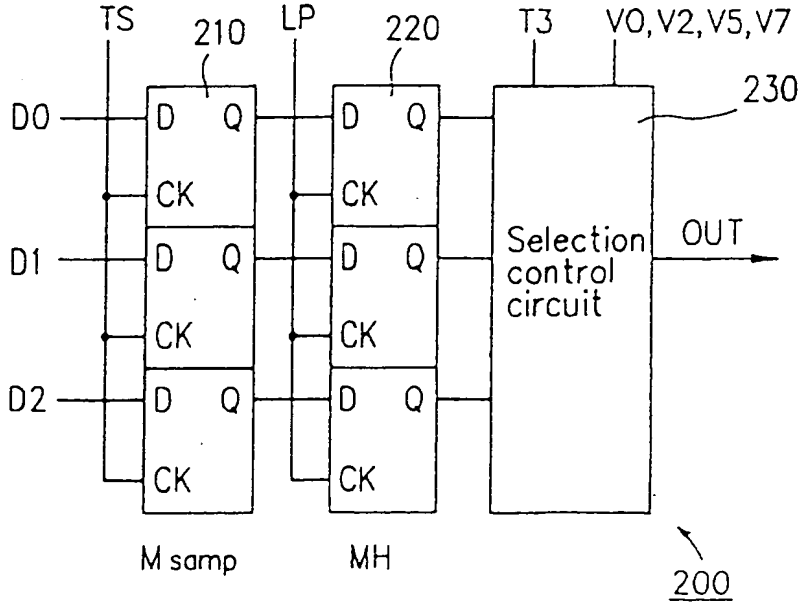


FIG.7 PRIOR ART

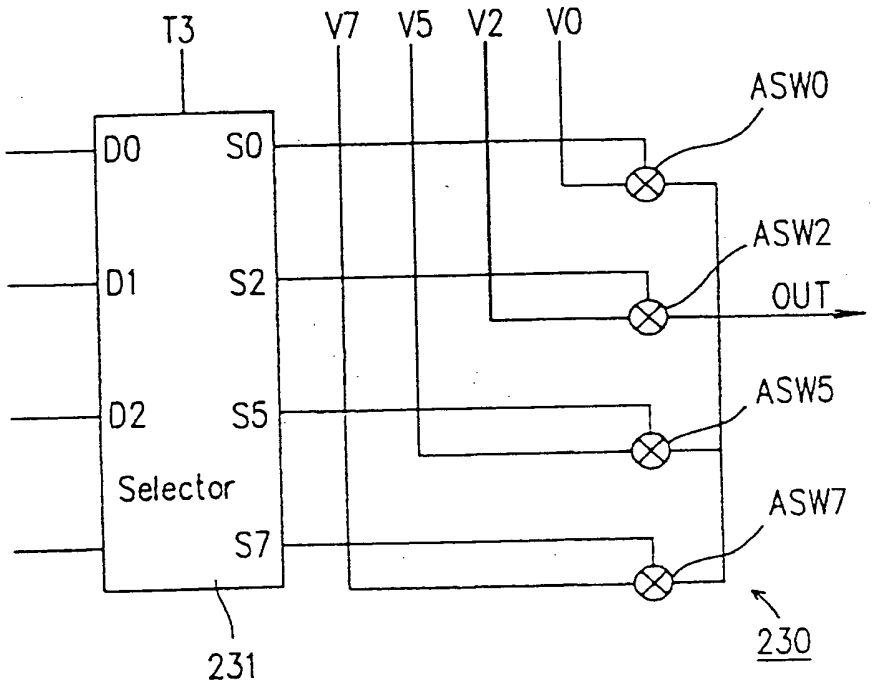
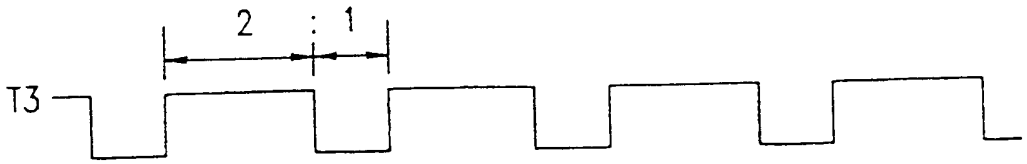


FIG.8 PRIOR ART

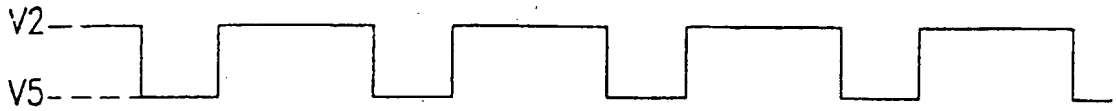


PRIOR ART

FIG.9A Output waveform when data is "1"

PRIOR ART

FIG.9B Output waveform when data is "3"



PRIOR ART

FIG.9C Output waveform when data is "4"

PRIOR ART

FIG.9D Output waveform when data is "6"

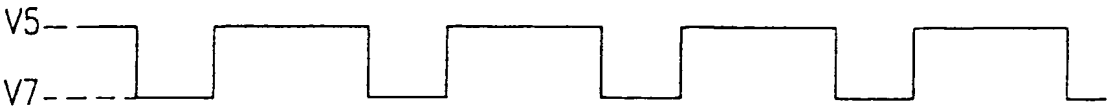


FIG.10 *PRIOR ART*

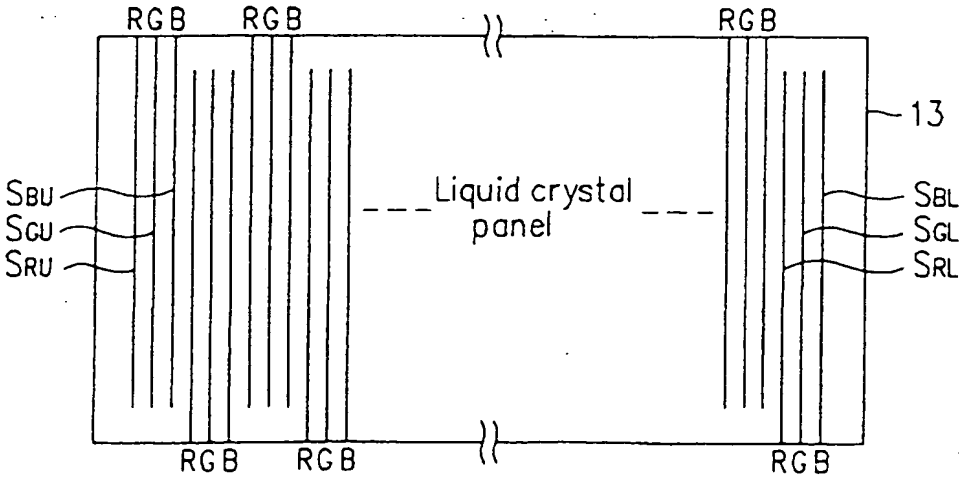


FIG.11 PRIOR ART

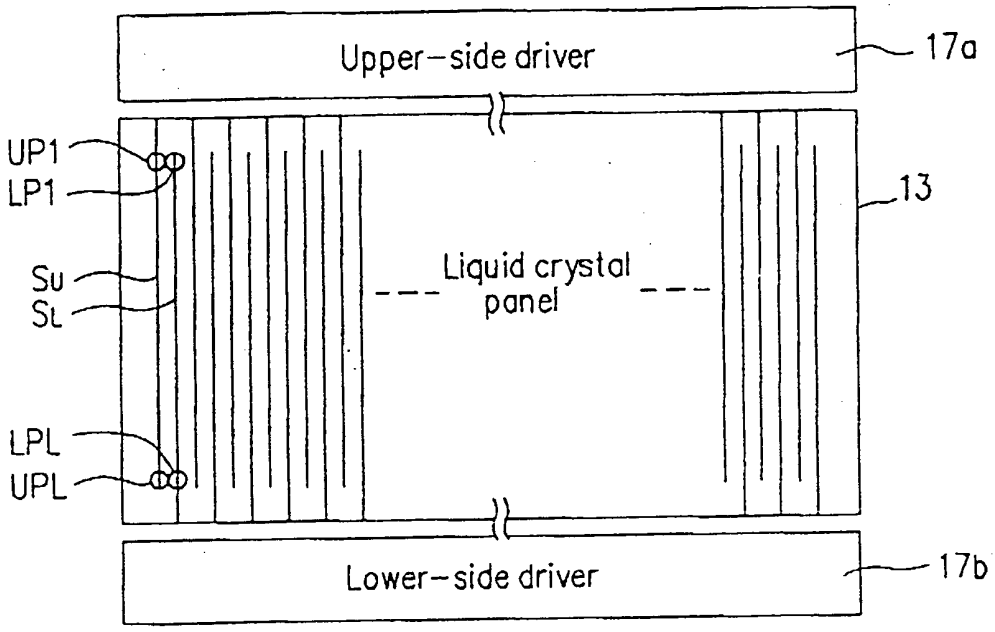


FIG.12

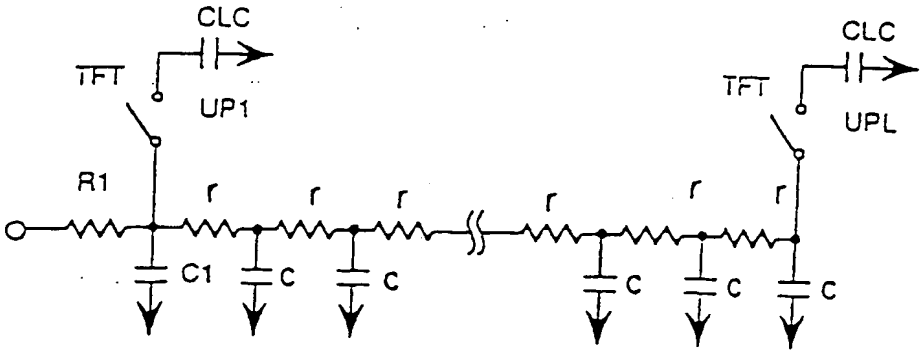


FIG.13A

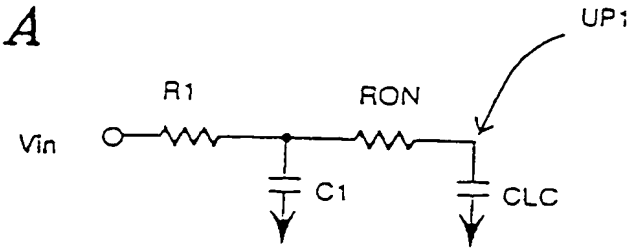
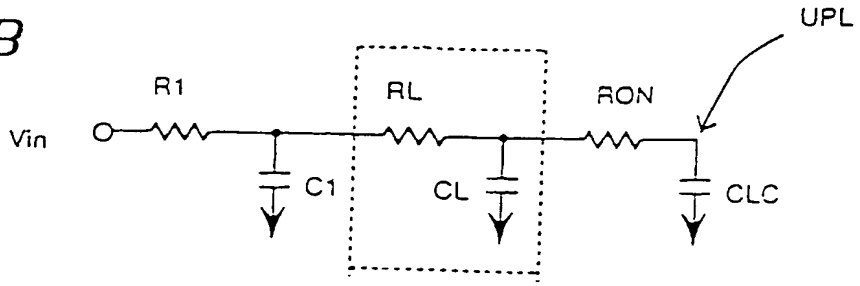


FIG.13B



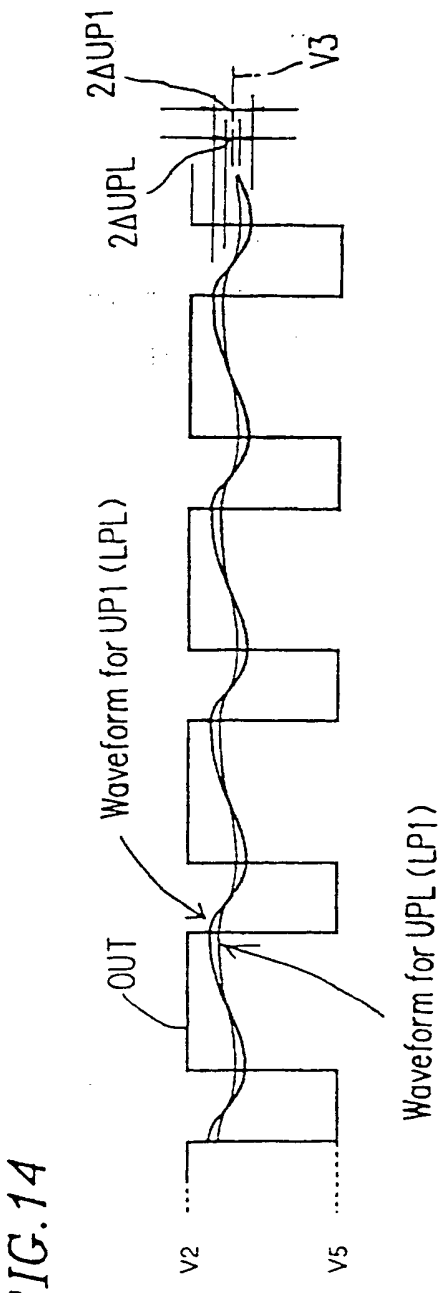

2ΔUP1
V3
2ΔUPL
Waveform for UP1 (LPL)
OUT
Waveform for UPL (LP1)
V2
V5

FIG. 14

FIG.15

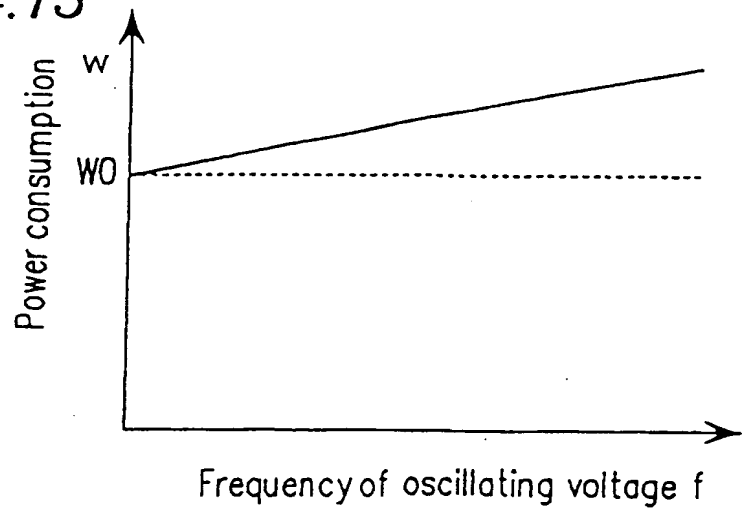

Power consumption
W
WO
Frequency of oscillating voltage f

FIG.16

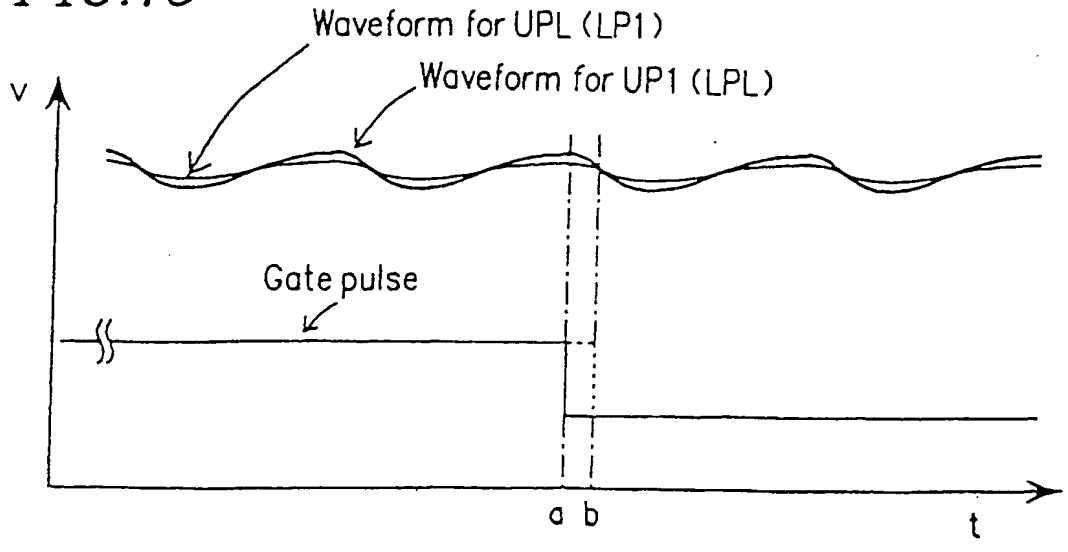

Waveform for UPL (LP1)
Waveform for UP1 (LPL)
V
Gate pulse
a b
t

FIG. 17

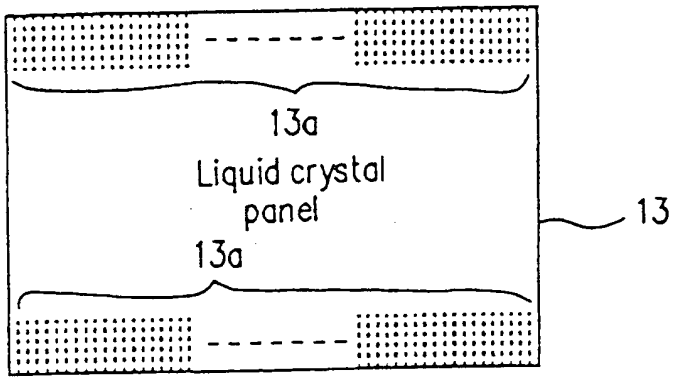


FIG.18

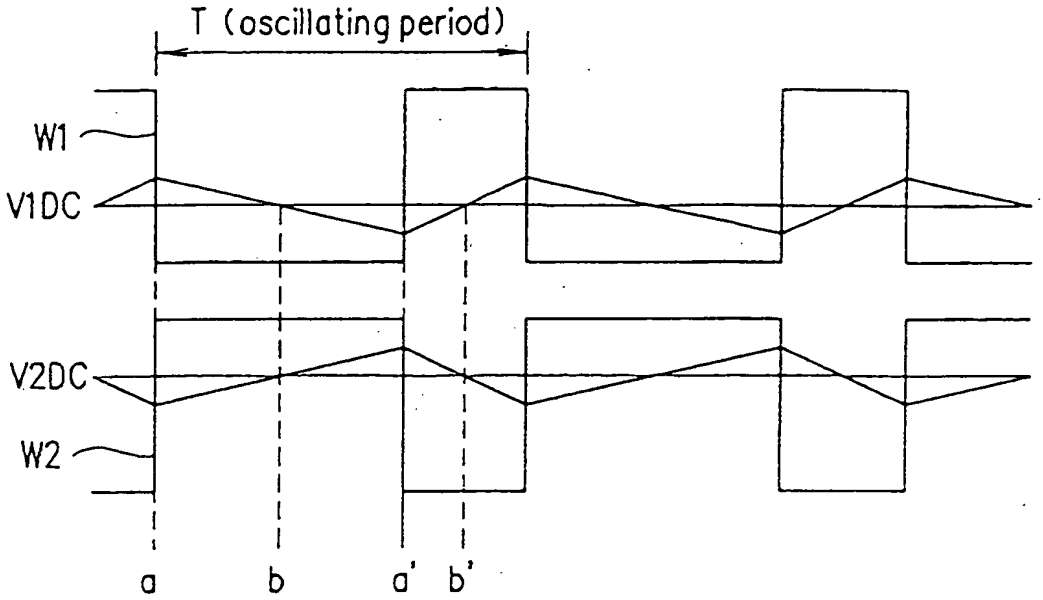

T (oscillating period)
W1
V1DC
V2DC
W2
a
b
a'
b'

FIG.19

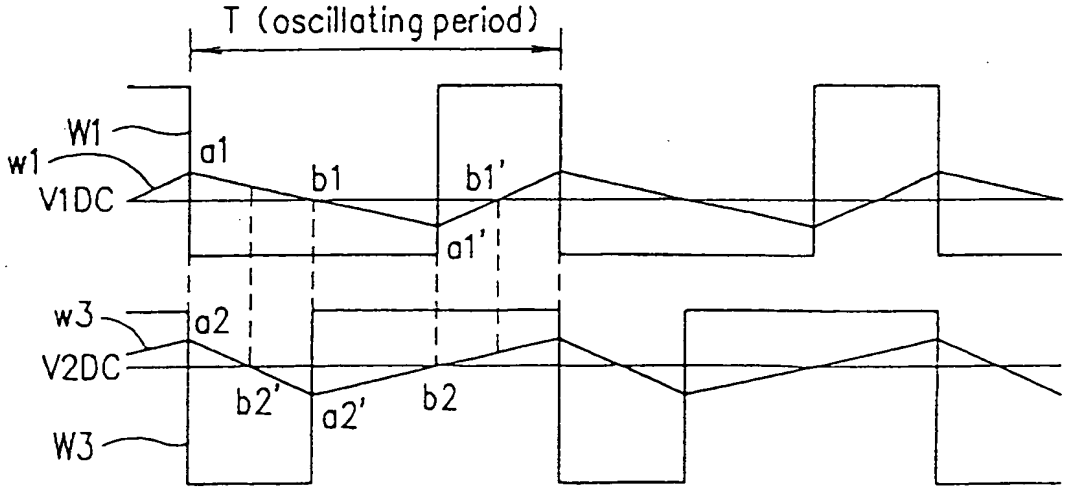

T (oscillating period)
W1
w1
V1DC
a1
b1
b1'
a1'
w3
V2DC
W3
a2
b2'
a2'
b2

FIG. 20

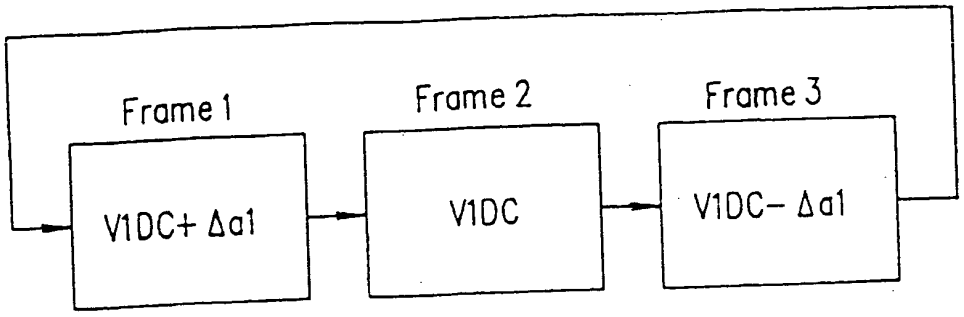

Frame 1
Frame 2
Frame 3
V1DC+ Δa1
V1DC
V1DC− Δa1

FIG. 21

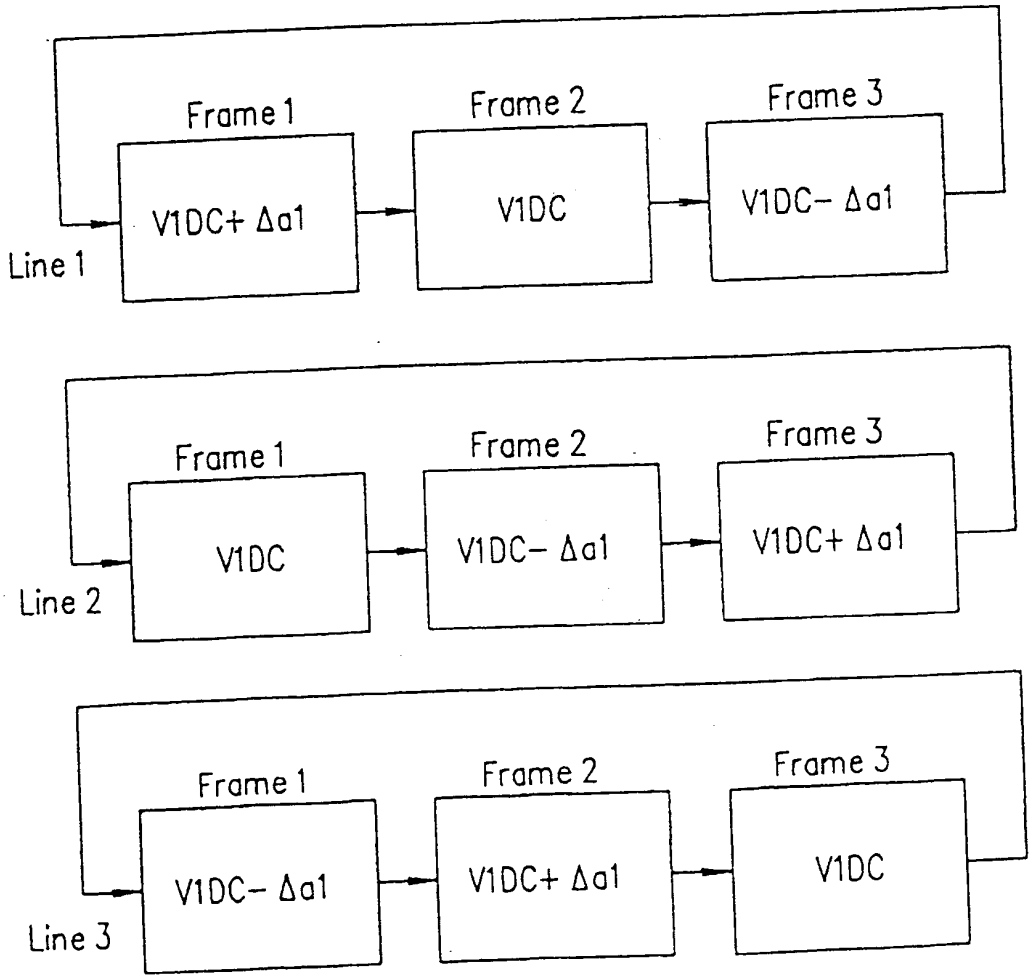
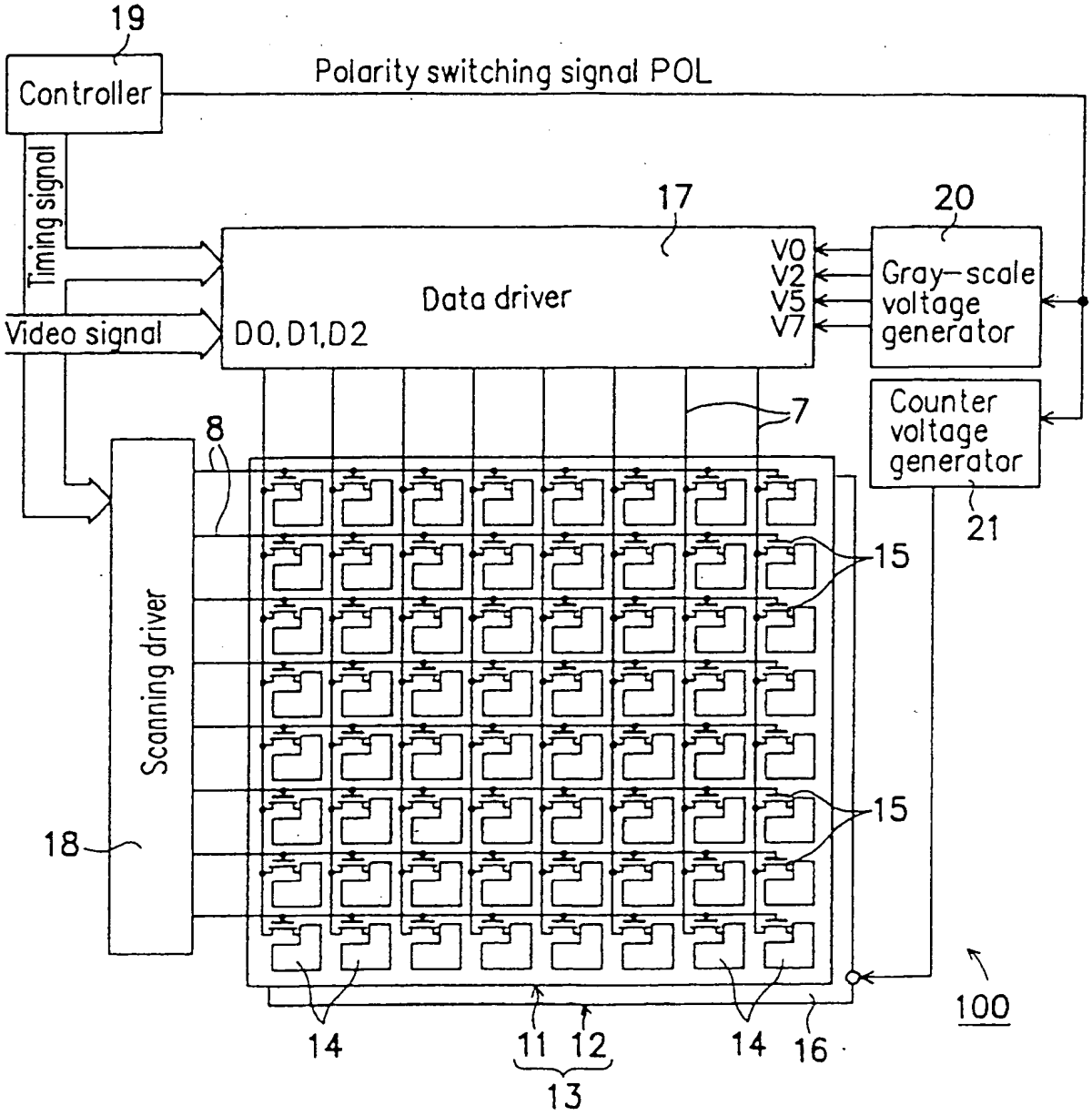

Frame 1
Frame 2
Frame 3
V1DC+ Δa1
V1DC
V1DC− Δa1
Line 1
Frame 1
Frame 2
Frame 3
V1DC
V1DC− Δa1
V1DC+ Δa1
Line 2
Frame 1
Frame 2
Frame 3
V1DC− Δa1
V1DC+ Δa1
V1DC
Line 3

FIG. 22


19
Controller
Polarity switching signal POL
Timing signal
17
20
Data driver
V0
V2
V5
V7
Gray-scale voltage generator
Video signal
D0, D1, D2
7
8
Counter voltage generator
21
15
Scanning driver
18
15
100
14
11
12
14
16
13